FIG. 1

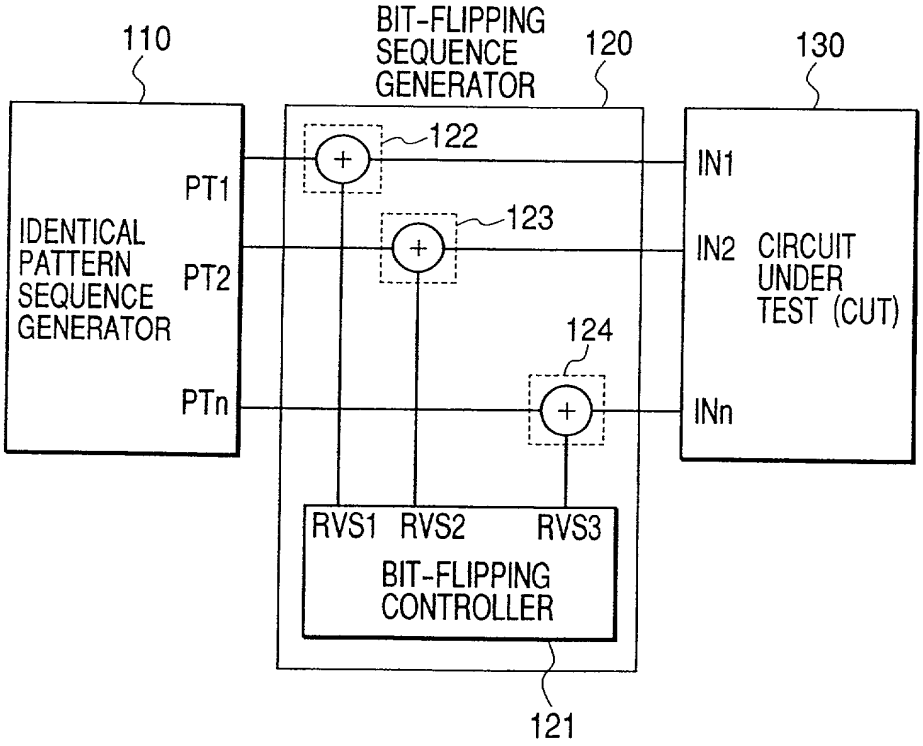

110
BIT-FLIPPING SEQUENCE GENERATOR
120
130
122
123
124
PT1
PT2
PTn
IDENTICAL PATTERN SEQUENCE GENERATOR
IN1
IN2
INn
CIRCUIT UNDER TEST (CUT)
RVS1
RVS2
RVS3
BIT-FLIPPING CONTROLLER
121

FIG. 2(a)

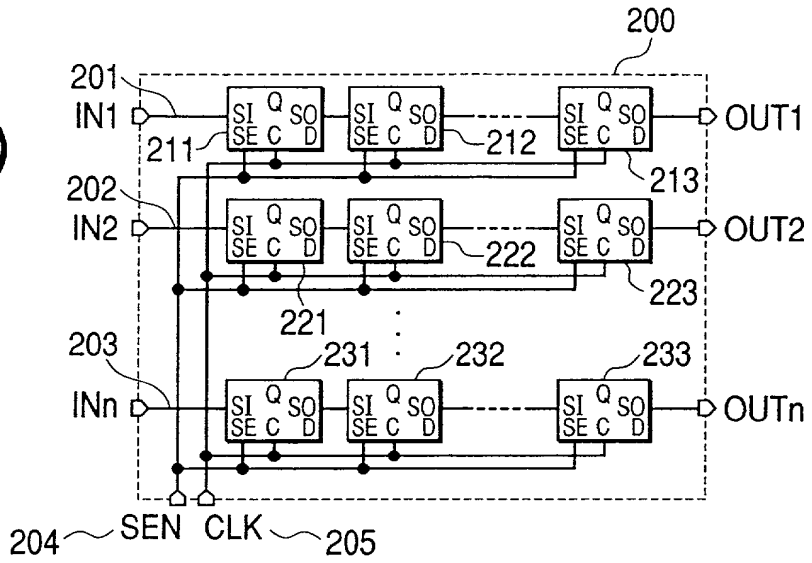


FIG. 2(b)

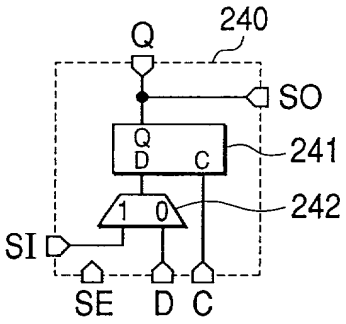


FIG. 2(c)

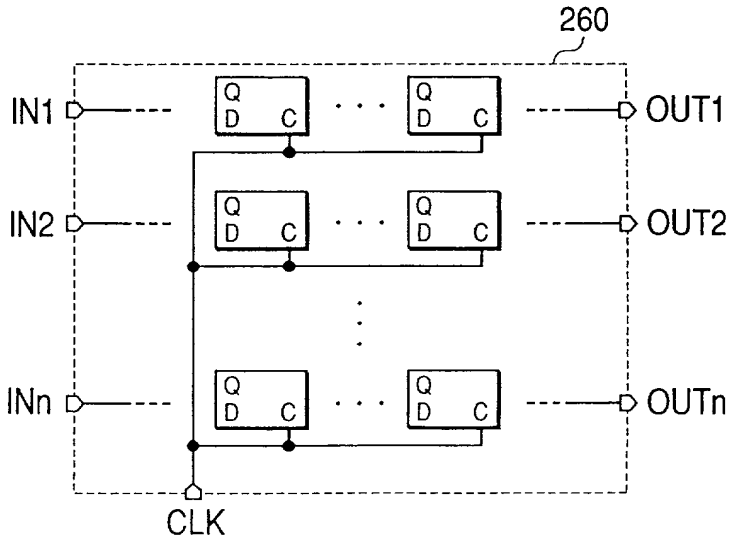


FIG. 3

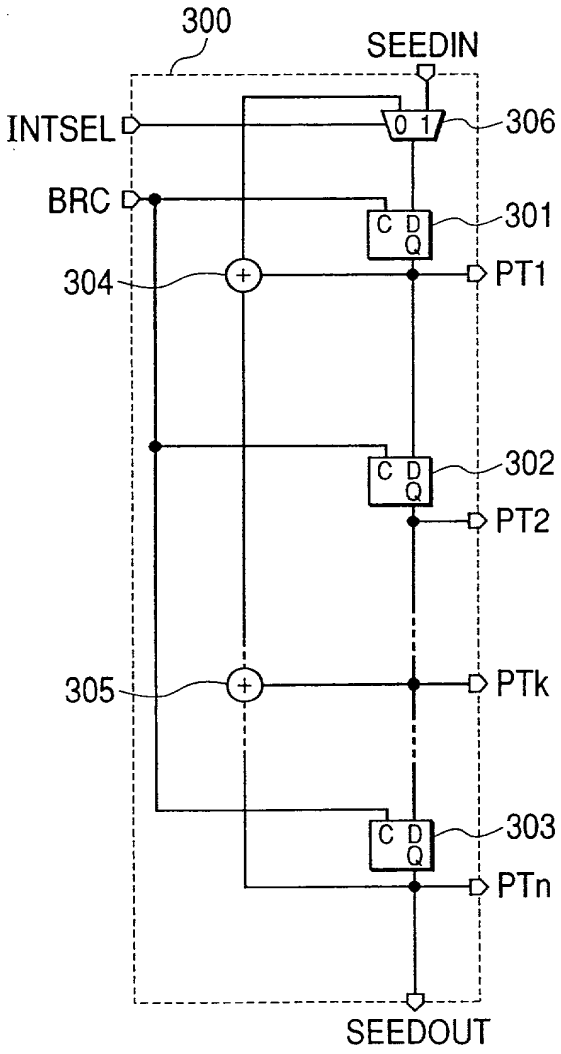

300
SEEDIN
INTSEL
BRC
304
305
306
301
302
303
PT1
PT2
PTk
PTn
SEEDOUT

FIG. 4

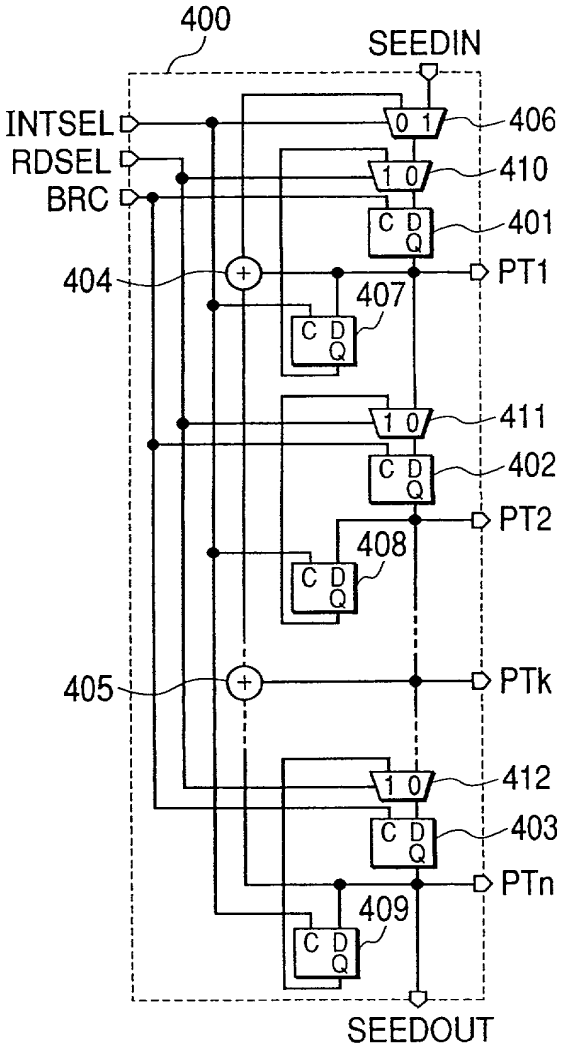

400
SEEDIN
INTSEL
RDSEL
BRC
404
405
406
410
401
407
411
402
408
412
403
409
PT1
PT2
PTk
PTn
SEEDOUT

FIG. 5

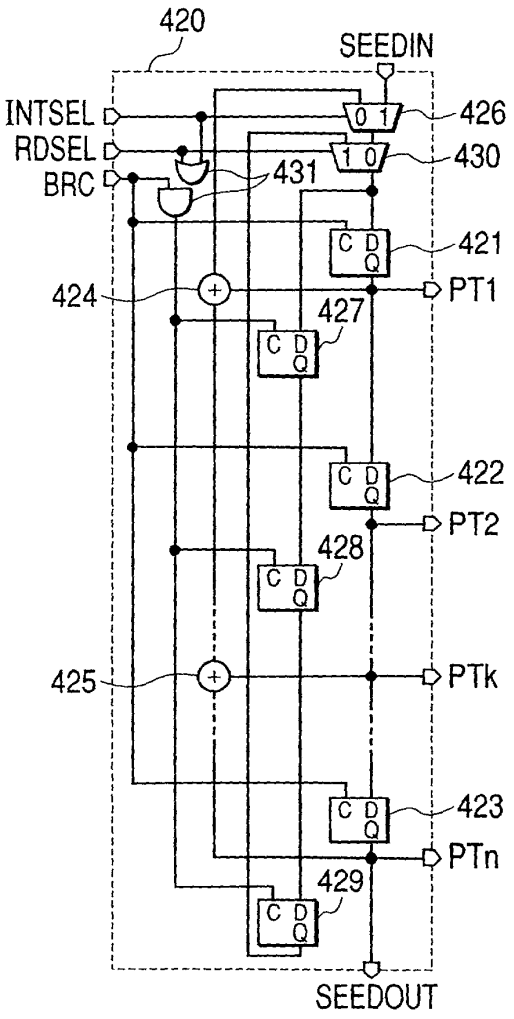

420
SEEDIN
INTSEL
RDSEL
BRC
426
430
431
421
424
PT1
427
422
PT2
428
425
PTk
423
PTn
429
SEEDOUT

FIG. 6

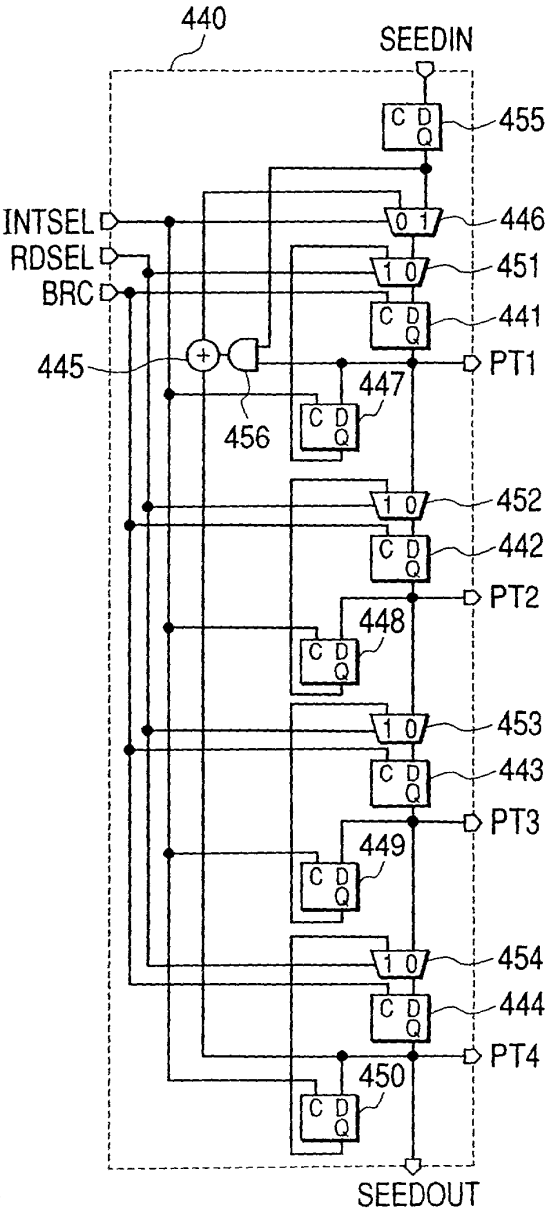

440
SEEDIN
455
INTSEL
RDSEL
BRC
446
451
441
445
PT1
447
456
452
442
PT2
448
453
443
PT3
449
454
444
PT4
450
SEEDOUT

FIG. 7

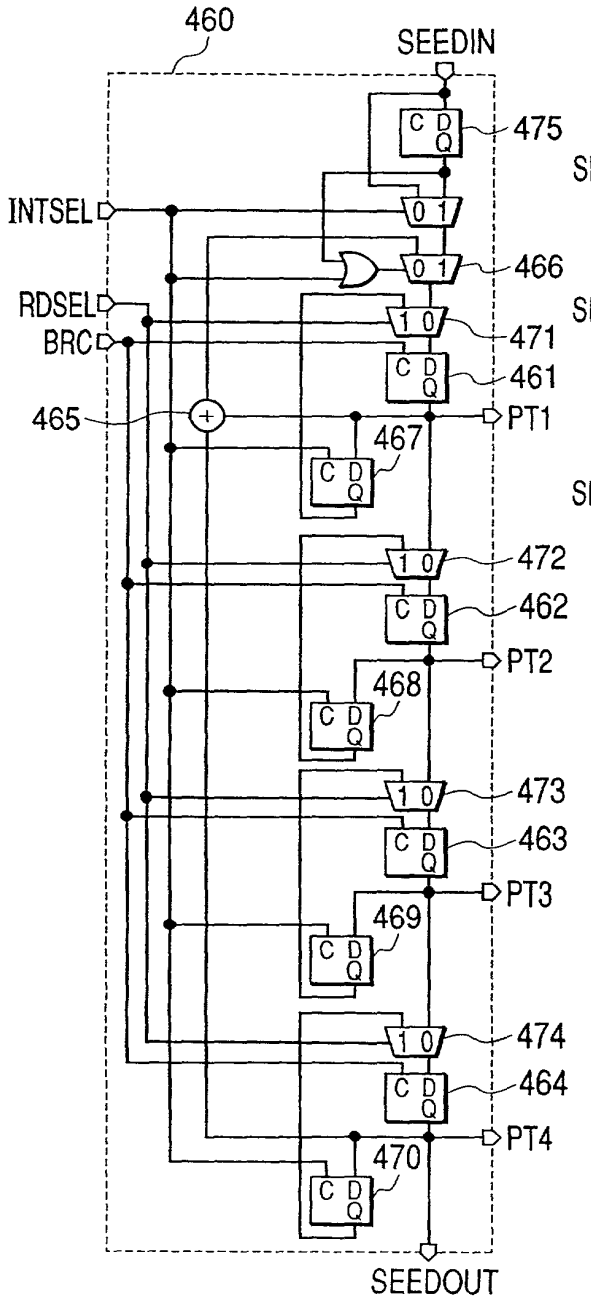

460
SEEDIN
475
INTSEL
466
RDSEL
BRC
471
461
465
PT1
467
472
462
PT2
468
473
463
PT3
469
474
464
PT4
470
SEEDOUT

FIG. 8

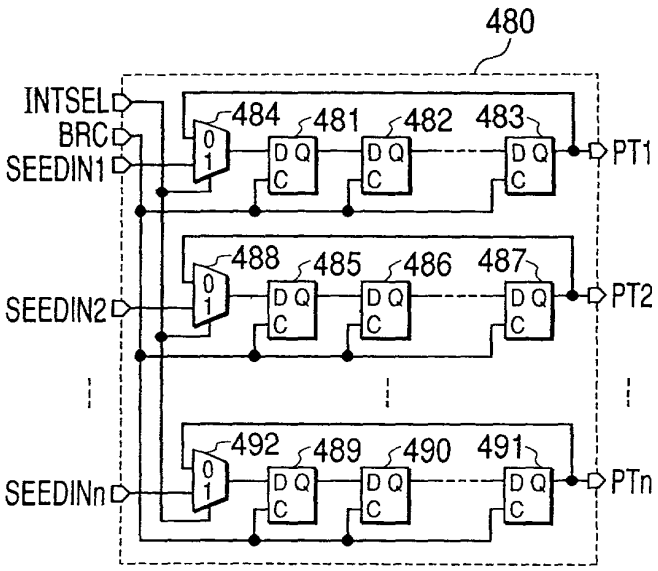

480
INTSEL
BRC
SEEDIN1
484
481
482
483
PT1
SEEDIN2
488
485
486
487
PT2
SEEDINn
492
489
490
491
PTn

FIG. 9(a)

MODE	INTSEL	BRC	REGISTER
INITIALIZATION	1	↑	SHIFT
PATTERN GENERATION	0	↑	RANDOM

FIG. 9(b)

MODE	INTSEL	RDSEL	BRC	REGISTER	SEED BACKUP REGISTER
INITIALIZATION	1	0	↑	SHIFT	SEED COPY
PATTERN GENERATION	0	0	↑	RANDOM	HOLD
SEED RECOVERY	0	1	↑	RECOVERY	HOLD
SEED UPDATE	1	0	—	—	SEED COPY

FIG. 9(c)

MODE	INTSEL	RDSEL	BRC	REGISTER	SEED BACKUP REGISTER
INITIALIZATION	1	0	↑	SHIFT	SEED COPY
PATTERN GENERATION	0	0	↑	RANDOM	HOLD
SEED RECOVERY	—	1	↑	RECOVERY	HOLD

FIG. 10

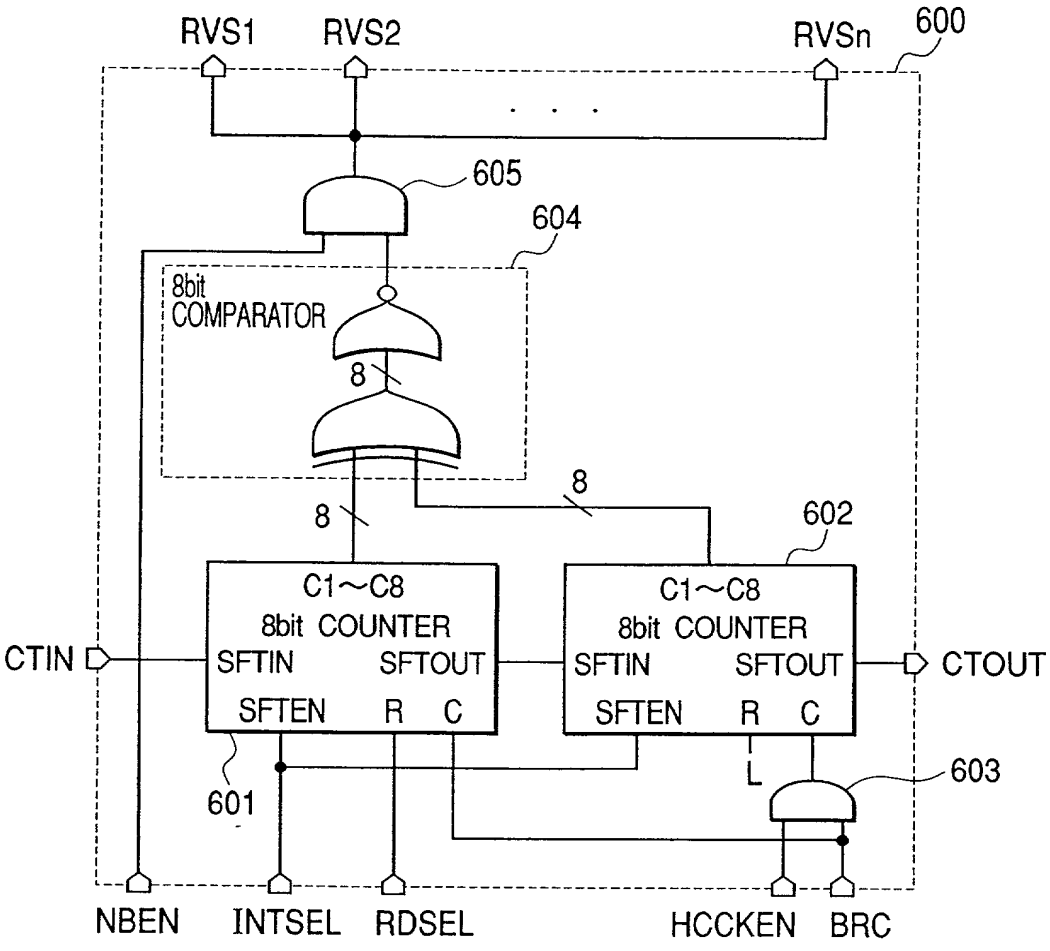

RVS1
RVS2
RVSn
600
605
604
8bit
COMPARATOR
8
8
8
602
C1~C8
8bit COUNTER
SFTIN
SFTOUT
SFTEN
R
C
C1~C8
8bit COUNTER
SFTIN
SFTOUT
SFTEN
R
C
CTIN
CTOUT
L
603
601
NBEN
INTSEL
RDSEL
HCCKEN
BRC

FIG. 11

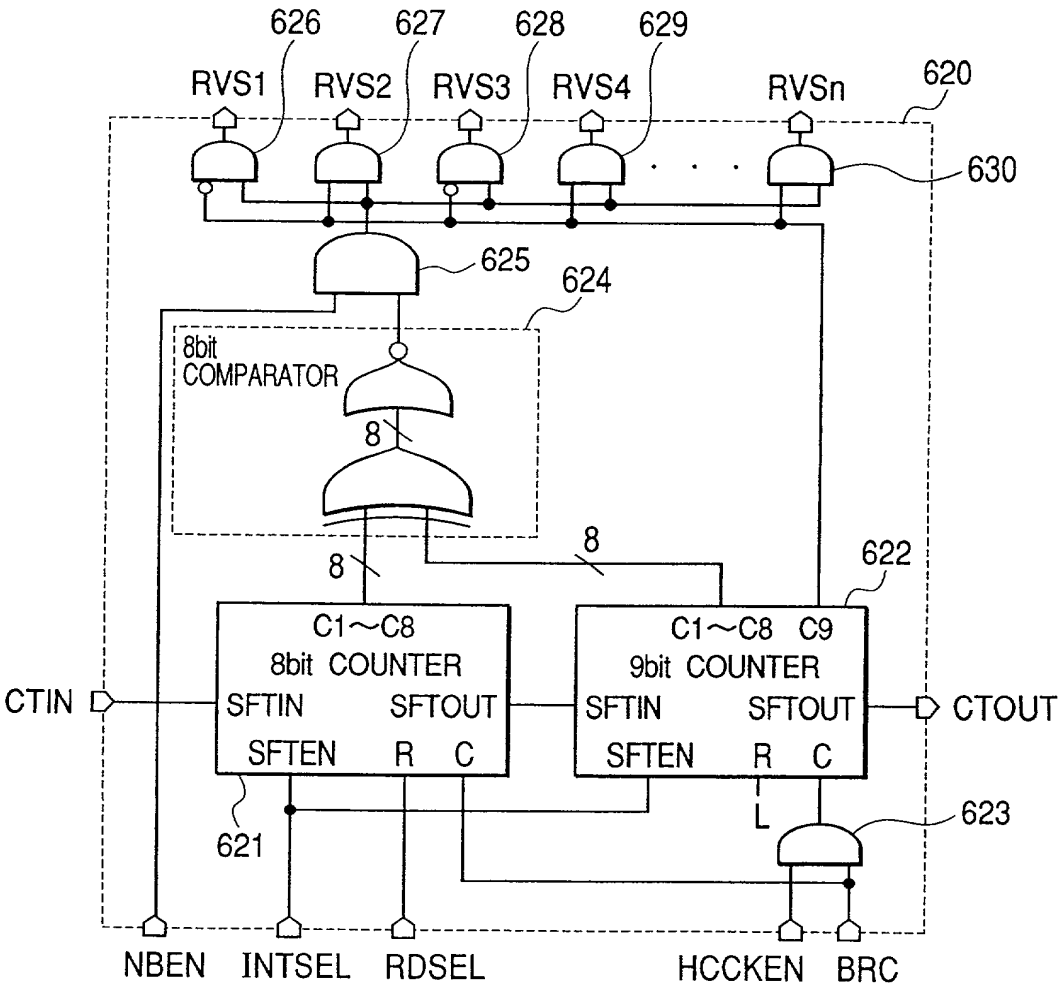

626
627
628
629
RVS1
RVS2
RVS3
RVS4
RVSn
620
630
625
624
8bit
COMPARATOR
8
8
8
622
C1~C8
8bit COUNTER
SFTIN
SFTOUT
SFTEN
R
C
C1~C8 C9
9bit COUNTER
SFTIN
SFTOUT
SFTEN
R
C
CTIN
CTOUT
L
623
621
NBEN
INTSEL
RDSEL
HCCKEN
BRC

FIG. 12

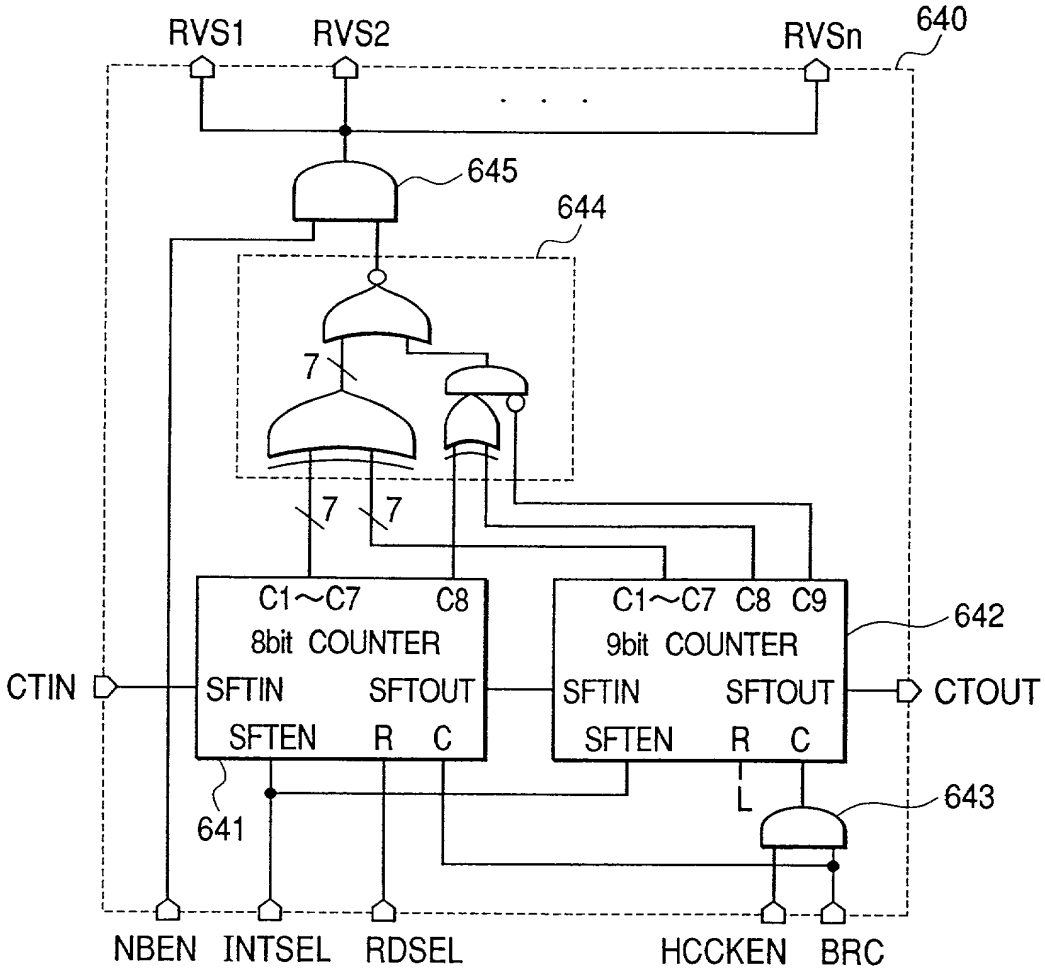

RVS1
RVS2
RVSn
640
645
644
7
7
7
C1~C7
C8
8bit COUNTER
SFTIN
SFTOUT
SFTEN
R
C
C1~C7
C8
C9
9bit COUNTER
SFTIN
SFTOUT
SFTEN
R
C
642
CTIN
CTOUT
L
643
641
NBEN
INTSEL
RDSEL
HCCKEN
BRC

FIG. 13

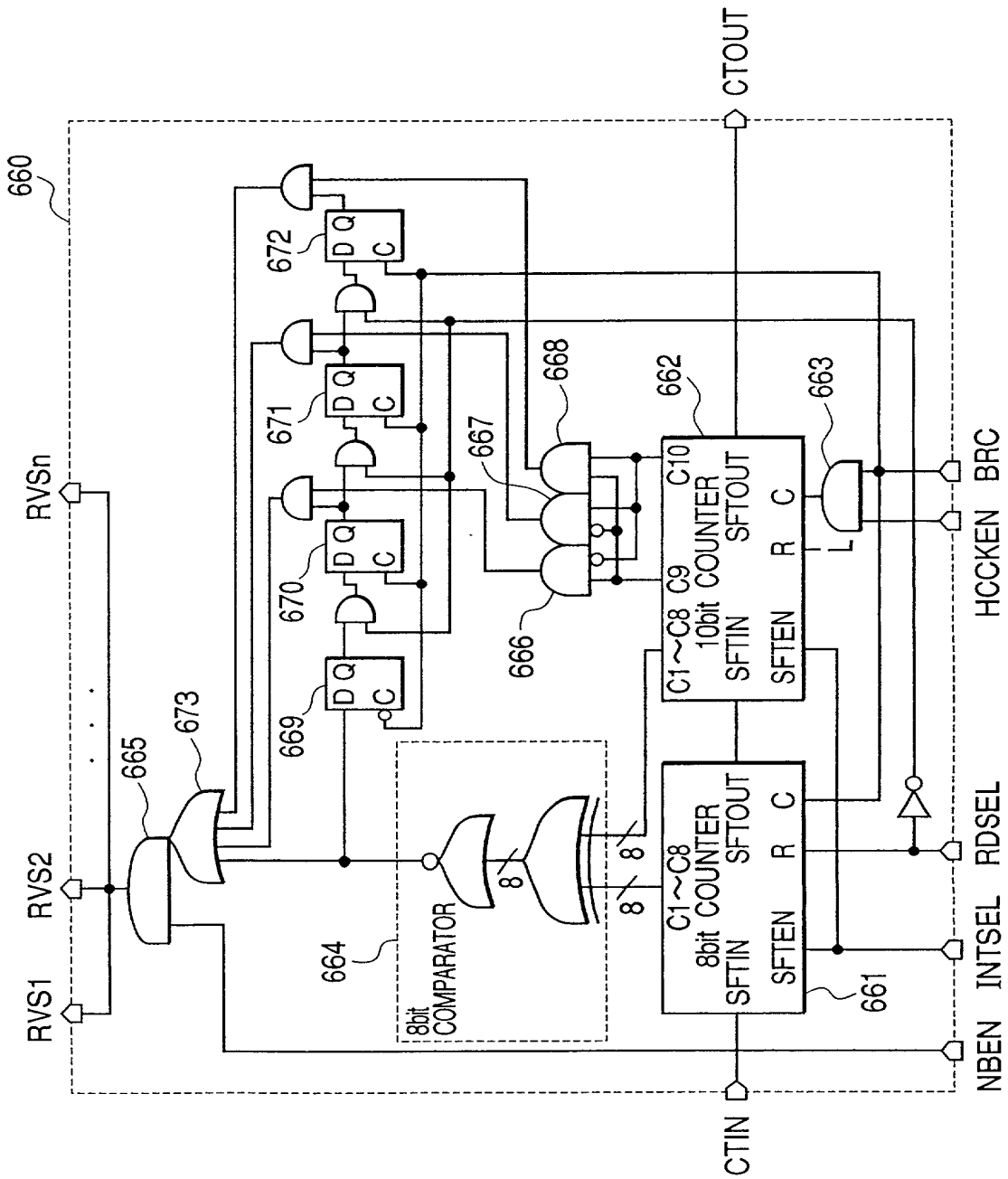
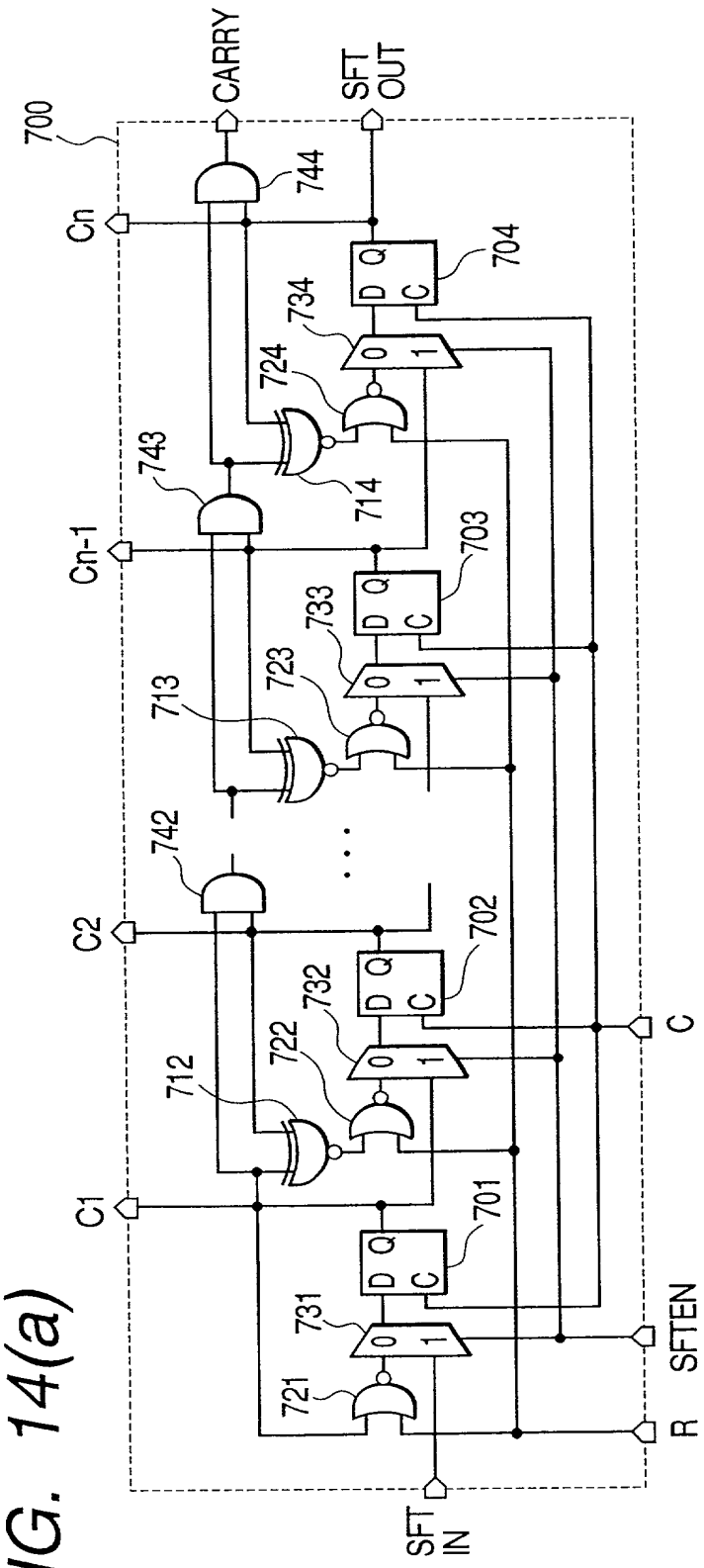

660
RVS1
RVS2
RVSn
CTIN
CTOUT
NBEN
INTSEL
RDSEL
HCCKEN
BRC
665
673
664
8bit COMPARATOR
669
670
671
672
666
667
668
662
C1~C8 C9 10bit COUNTER C10
SFTIN
SFTEN
SFTOUT
R
C
L
663
C1~C8 8bit COUNTER
661
D Q
C
8

FIG. 14(a)



MODE	SFTEN	R	C
SHIFT	1	0	↑
RESET	0	1	↑
INCREMENT	0	0	↑

FIG. 14(b)

FIG. 15(a)

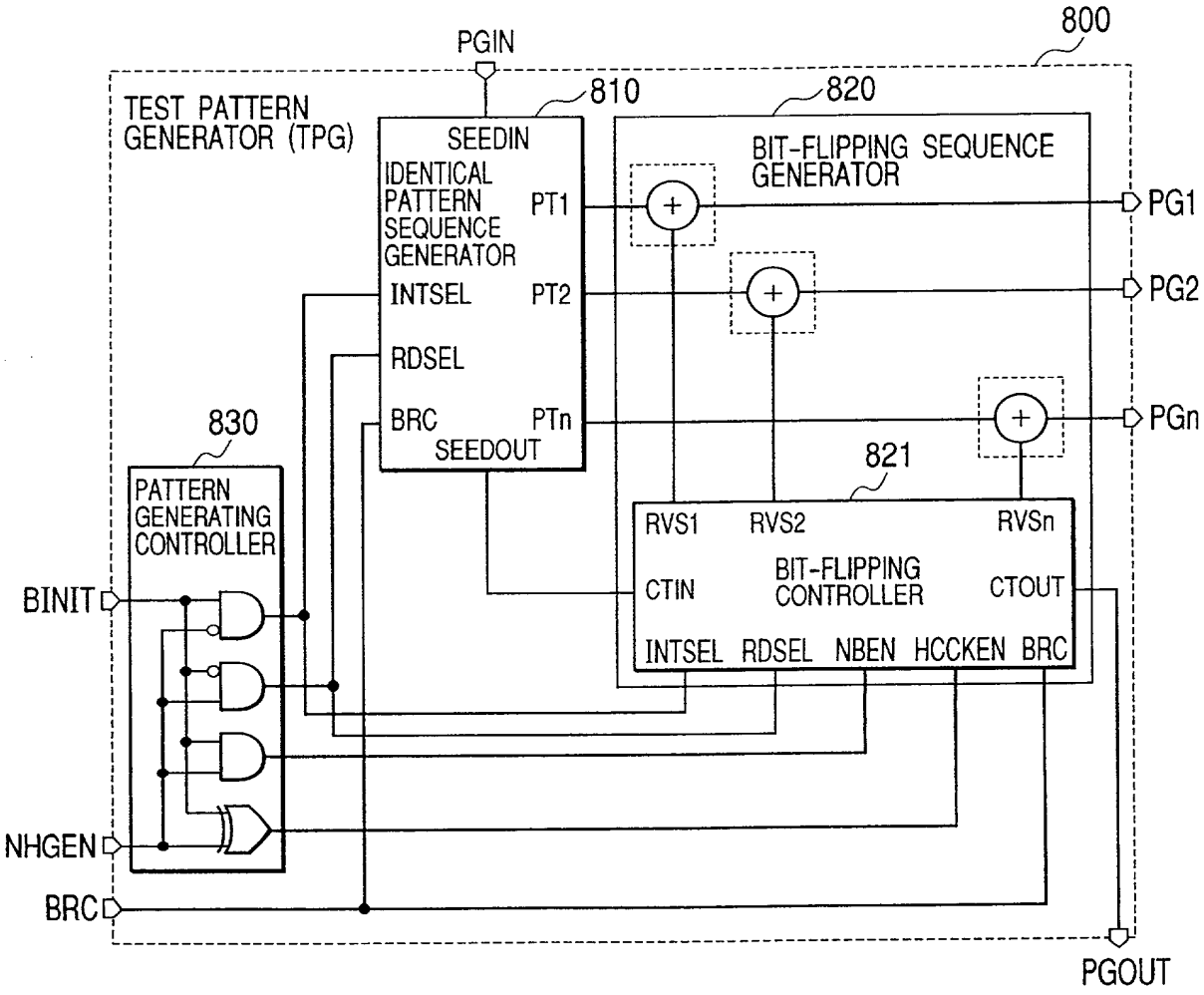


FIG. 15(b)

	MODE	BINIT	NHGEN	INTSEL	RDSEL	NBEN	HCCKEN
841	INITIALIZATION	1	0	1	0	0	1
842	PATTERN GENERATION	0	0	0	0	0	0
843	SEED RECOVERY	0	1	0	1	0	1
844	NEIGHBORHOOD PATTERN GENERATION	1	1	0	0	1	0

FIG. 16

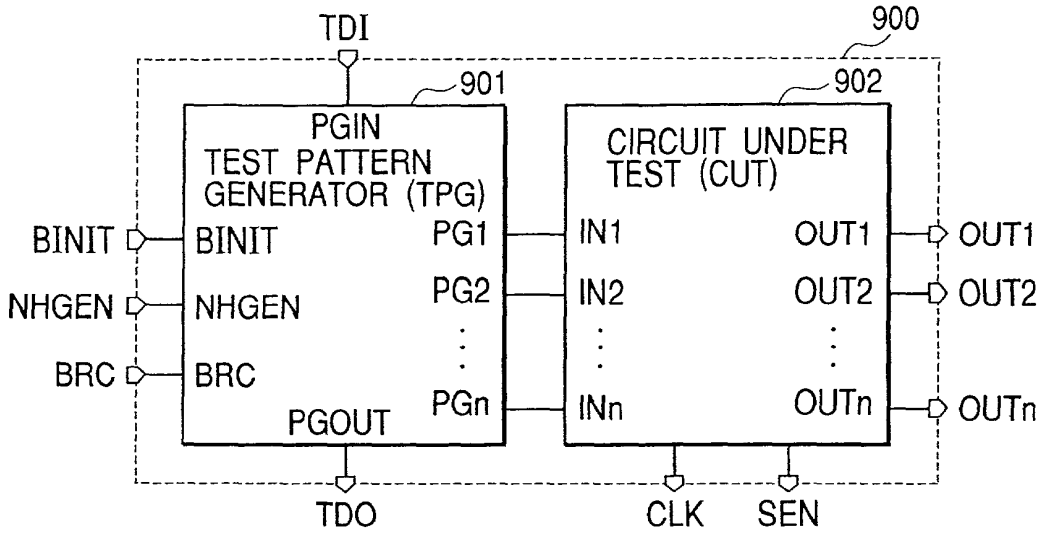

TDI
900
901
902
PGIN
TEST PATTERN
GENERATOR (TPG)
CIRCUIT UNDER
TEST (CUT)
BINIT
NHGEN
BRC
PG1
PG2
PGn
PGOUT
IN1
IN2
INn
OUT1
OUT2
OUTn
TDO
CLK
SEN

FIG. 17

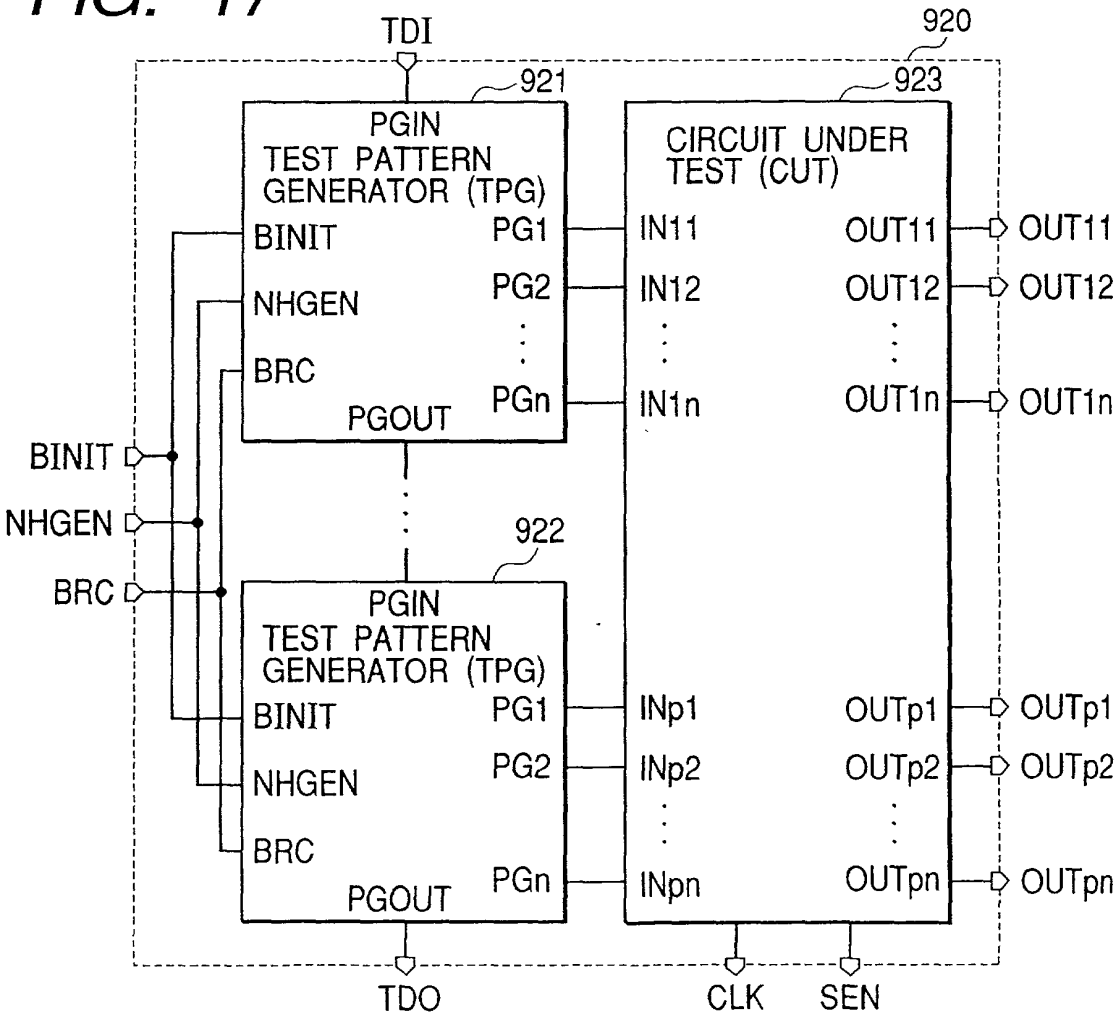

TDI
920
921
923
922
PGIN
TEST PATTERN
GENERATOR (TPG)
CIRCUIT UNDER
TEST (CUT)
BINIT
NHGEN
BRC
PG1
PG2
PGn
PGOUT
IN11
IN12
IN1n
OUT11
OUT12
OUT1n
INp1
INp2
INpn
OUTp1
OUTp2
OUTpn
TDO
CLK
SEN

FIG. 18

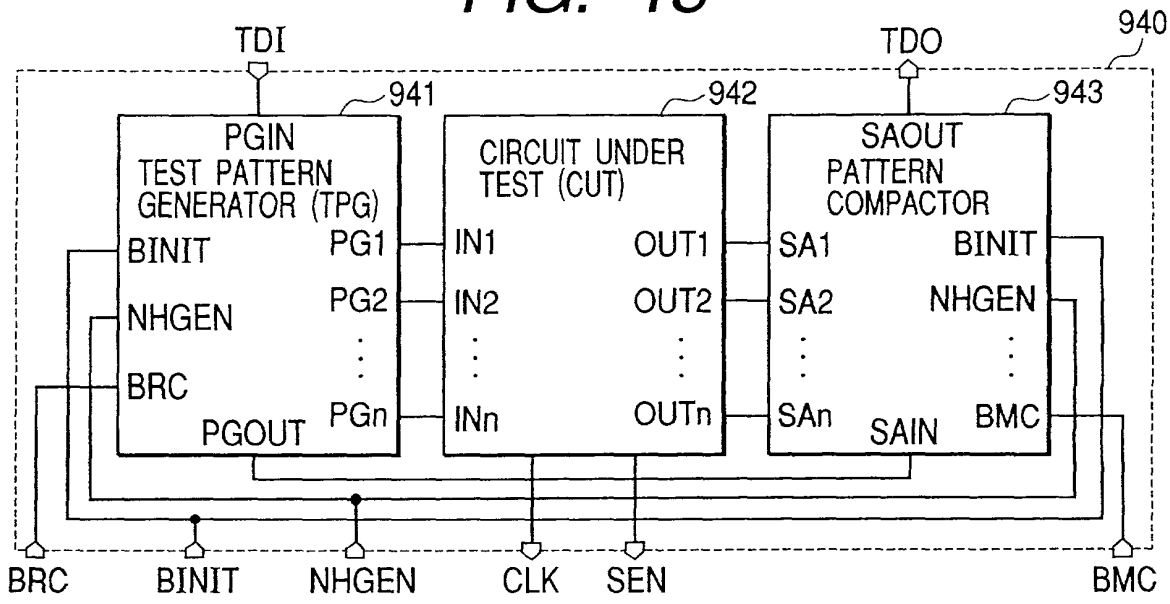

TDI
TDO
940
941
942
943
PGIN
TEST PATTERN
GENERATOR (TPG)
BINIT
NHGEN
BRC
PGOUT
PG1
PG2
PGn
CIRCUIT UNDER
TEST (CUT)
IN1
IN2
INn
OUT1
OUT2
OUTn
SAOUT
PATTERN
COMPACTOR
SA1
SA2
SAn
SAIN
BINIT
NHGEN
BMC
BRC
BINIT
NHGEN
CLK
SEN
BMC

FIG. 19

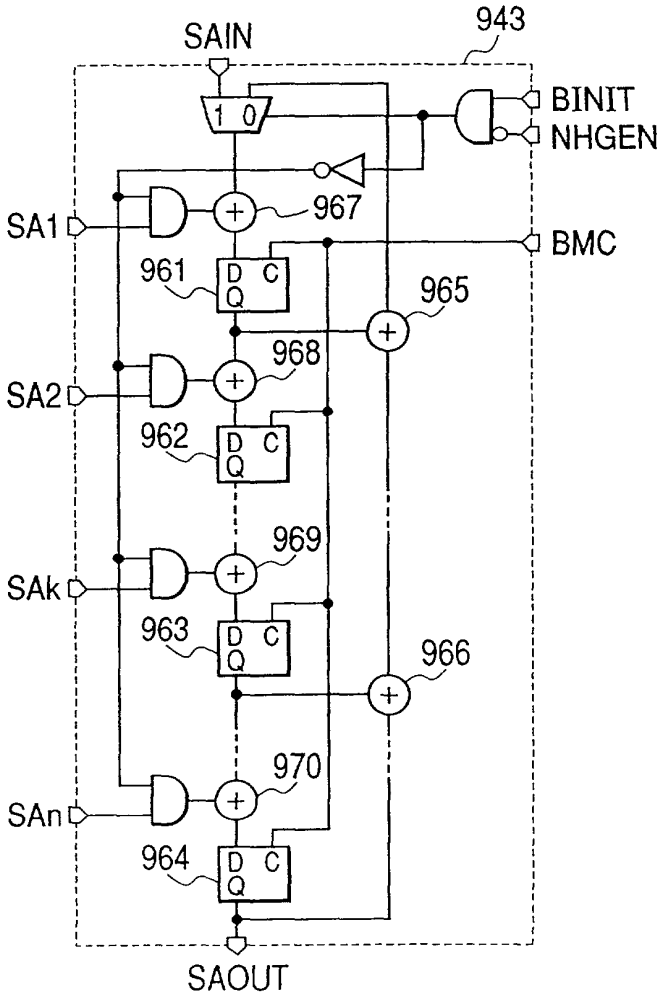

SAIN
943
1 0
BINIT
NHGEN
967
SA1
BMC
961
D C
Q
965
968
SA2
962
969
SAk
963
966
970
SAn
964
SAOUT

FIG. 20

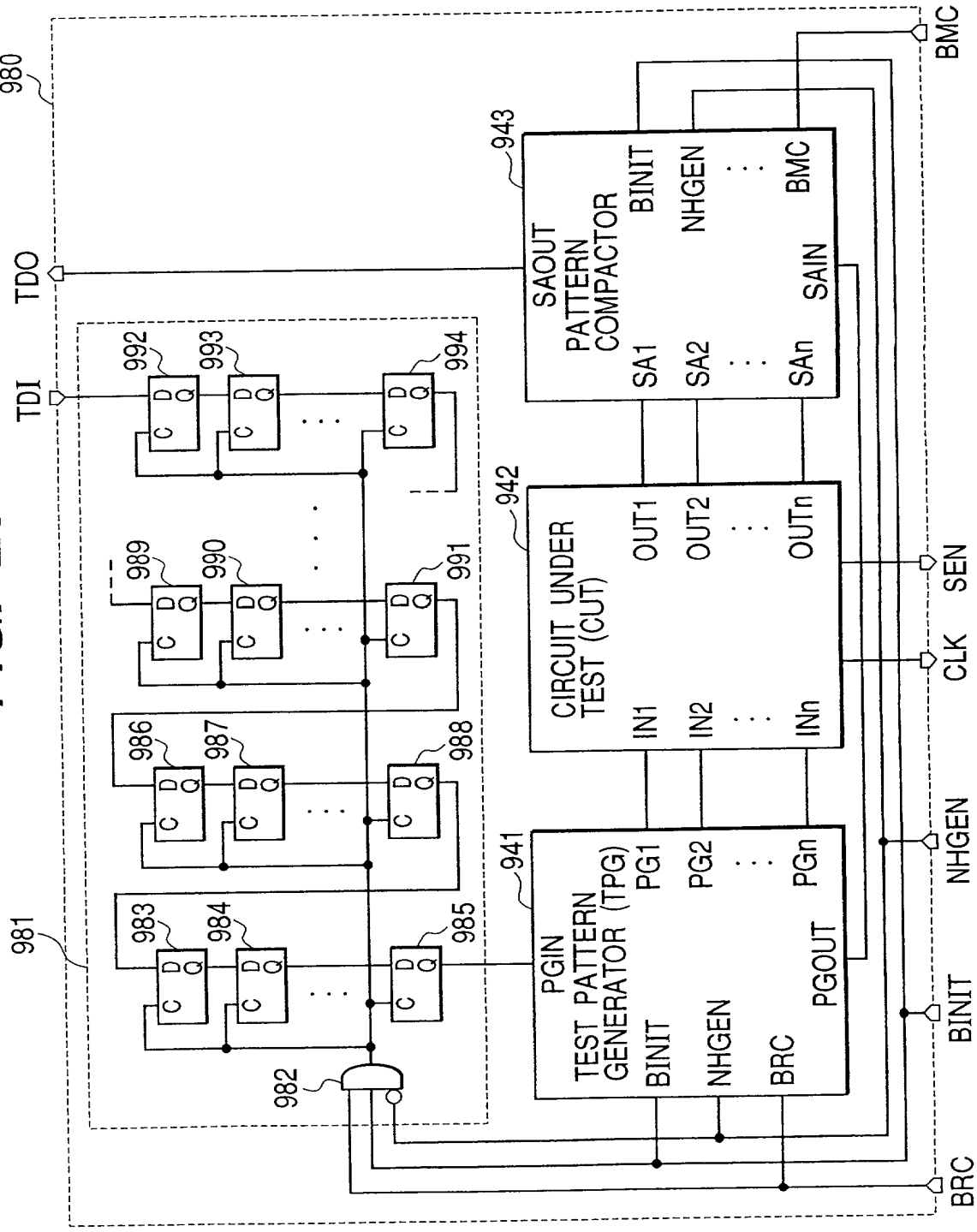

980
TDI
TDO
981
982
983
984
985
986
987
988
989
990
991
992
993
994
941
PGIN
TEST PATTERN GENERATOR (TPG)
BINIT
NHGEN
BRC
PG1
PG2
PGn
PGOUT
942
CIRCUIT UNDER TEST (CUT)
IN1
IN2
INn
OUT1
OUT2
OUTn
943
SAOUT
PATTERN COMPACTOR
SA1
SA2
SAn
SAIN
BINIT
NHGEN
BMC
BMC
SEN
CLK
NHGEN
BINIT
BRC

FIG. 21

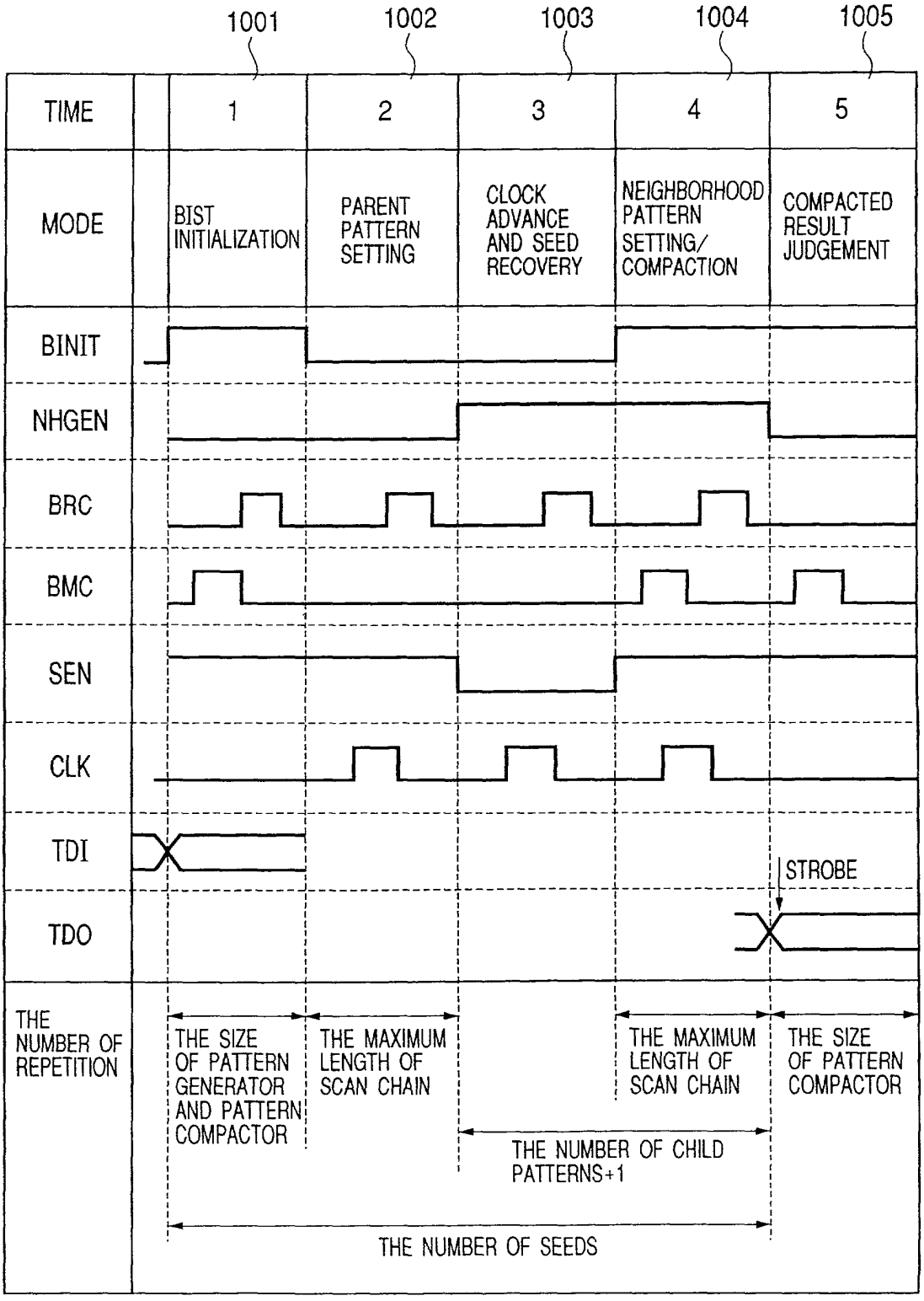

1001
1002
1003
1004
1005
TIME
1
2
3
4
5
MODE
BIST INITIALIZATION
PARENT PATTERN SETTING
CLOCK ADVANCE AND SEED RECOVERY
NEIGHBORHOOD PATTERN SETTING/ COMPACTION
COMPACTED RESULT JUDGEMENT
BINIT
NHGEN
BRC
BMC
SEN
CLK
TDI
STROBE
TDO
THE NUMBER OF REPETITION
THE SIZE OF PATTERN GENERATOR AND PATTERN COMPACTOR
THE MAXIMUM LENGTH OF SCAN CHAIN
THE MAXIMUM LENGTH OF SCAN CHAIN
THE SIZE OF PATTERN COMPACTOR
THE NUMBER OF CHILD PATTERNS+1
THE NUMBER OF SEEDS

FIG. 22

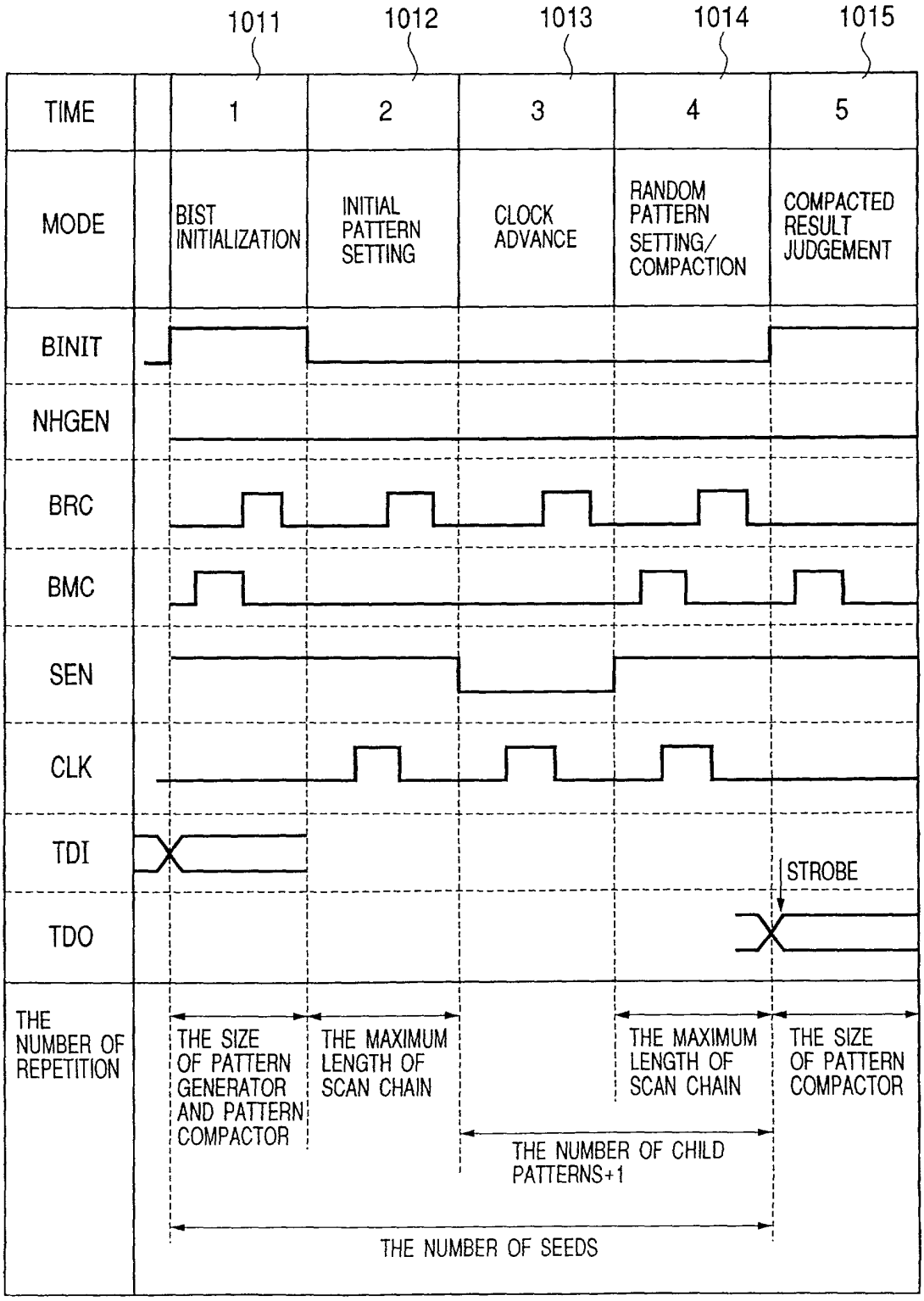

1011
1012
1013
1014
1015
TIME
1
2
3
4
5
MODE
BIST INITIALIZATION
INITIAL PATTERN SETTING
CLOCK ADVANCE
RANDOM PATTERN SETTING/ COMPACTION
COMPACTED RESULT JUDGEMENT
BINIT
NHGEN
BRC
BMC
SEN
CLK
TDI
STROBE
TDO
THE NUMBER OF REPETITION
THE SIZE OF PATTERN GENERATOR AND PATTERN COMPACTOR
THE MAXIMUM LENGTH OF SCAN CHAIN
THE MAXIMUM LENGTH OF SCAN CHAIN
THE SIZE OF PATTERN COMPACTOR
THE NUMBER OF CHILD PATTERNS+1
THE NUMBER OF SEEDS

FIG. 23

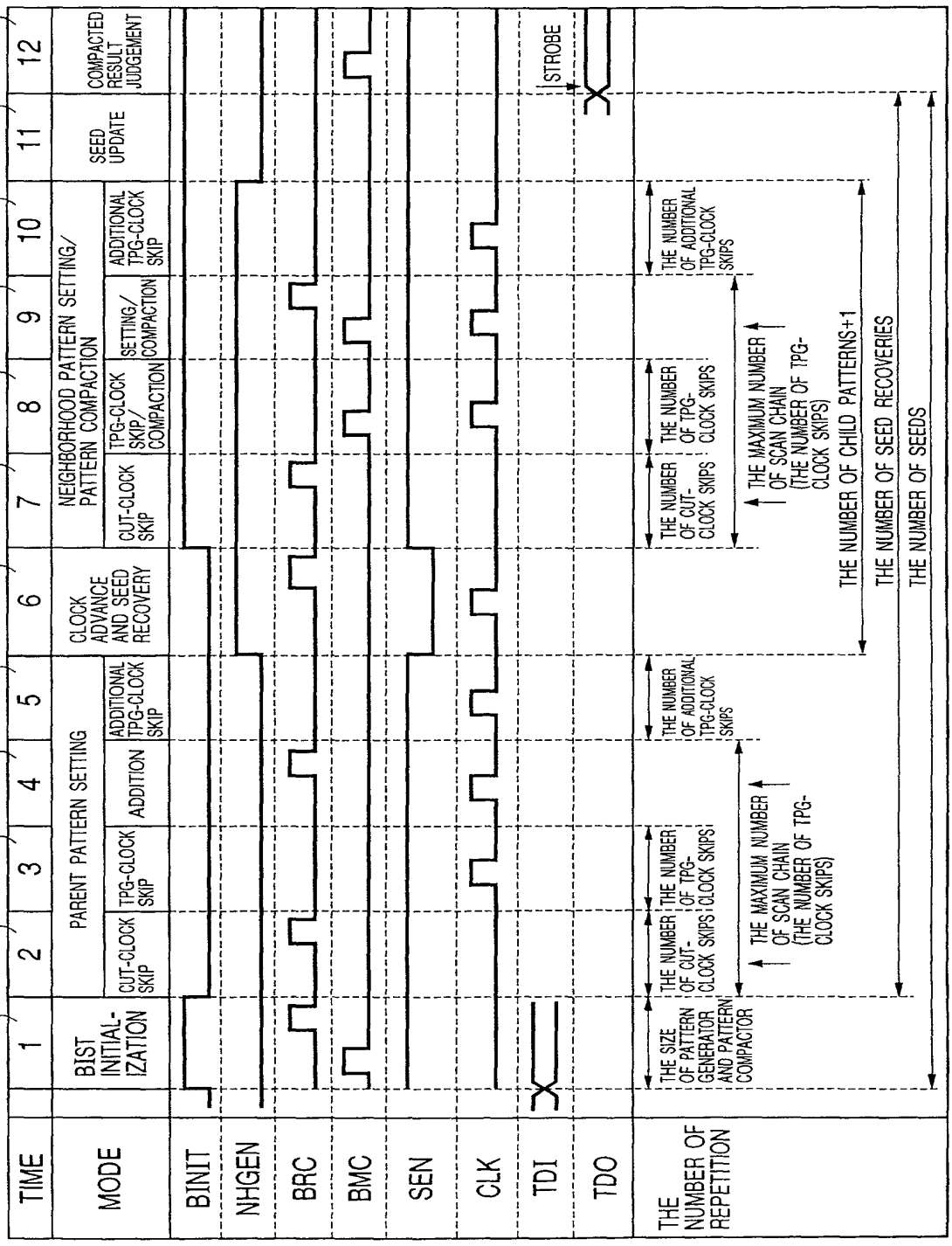

TIME
MODE
1021
1022
1023
1024
1025
1026
1027
1028
1029
1030
1031
1032
1
2
3
4
5
6
7
8
9
10
11
12
BIST INITIAL-IZATION
PARENT PATTERN SETTING
CUT-CLOCK SKIP
TPG-CLOCK SKIP
ADDITION
ADDITIONAL TPG-CLOCK SKIP
CLOCK ADVANCE AND SEED RECOVERY
NEIGHBORHOOD PATTERN SETTING/ PATTERN COMPACTION
CUT-CLOCK SKIP
TPG-CLOCK SKIP/ COMPACTION
SETTING/ COMPACTION
ADDITIONAL TPG-CLOCK SKIP
SEED UPDATE
COMPACTED RESULT JUDGEMENT
BINIT
NHGEN
BRC
BMC
SEN
CLK
TDI
TDO
STROBE
THE NUMBER OF REPETITION
THE SIZE OF PATTERN GENERATOR AND PATTERN COMPACTOR
THE NUMBER OF CUT-CLOCK SKIPS
THE NUMBER OF TPG-CLOCK SKIPS
THE NUMBER OF ADDITIONAL TPG-CLOCK SKIPS
THE MAXIMUM NUMBER OF SCAN CHAIN (THE NUMBER OF TPG-CLOCK SKIPS)
THE NUMBER OF CHILD PATTERNS+1
THE NUMBER OF SEED RECOVERIES
THE NUMBER OF SEEDS

FIG. 24

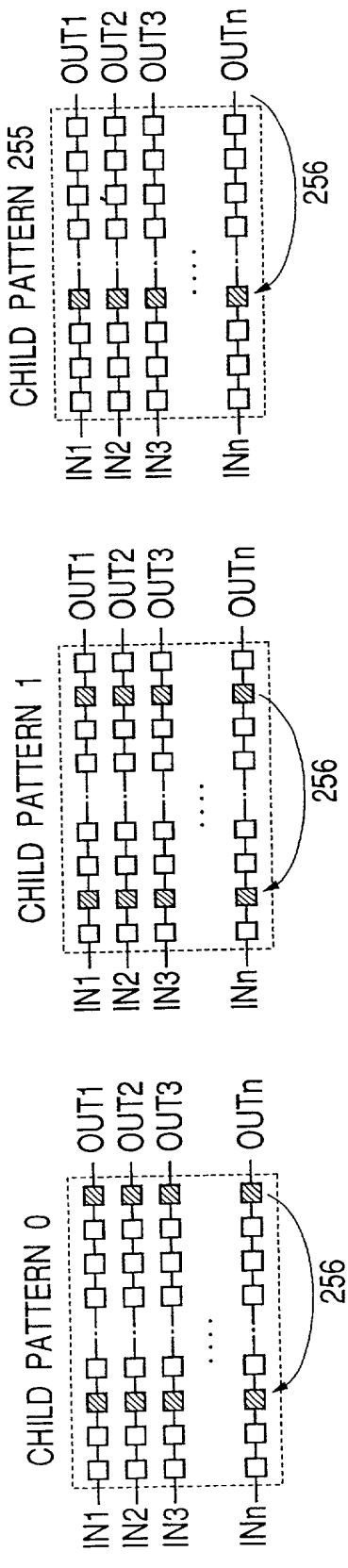

CHILD PATTERN 0
CHILD PATTERN 1
CHILD PATTERN 255
IN1
IN2
IN3
INn
OUT1
OUT2
OUT3
OUTn
256

FIG. 25

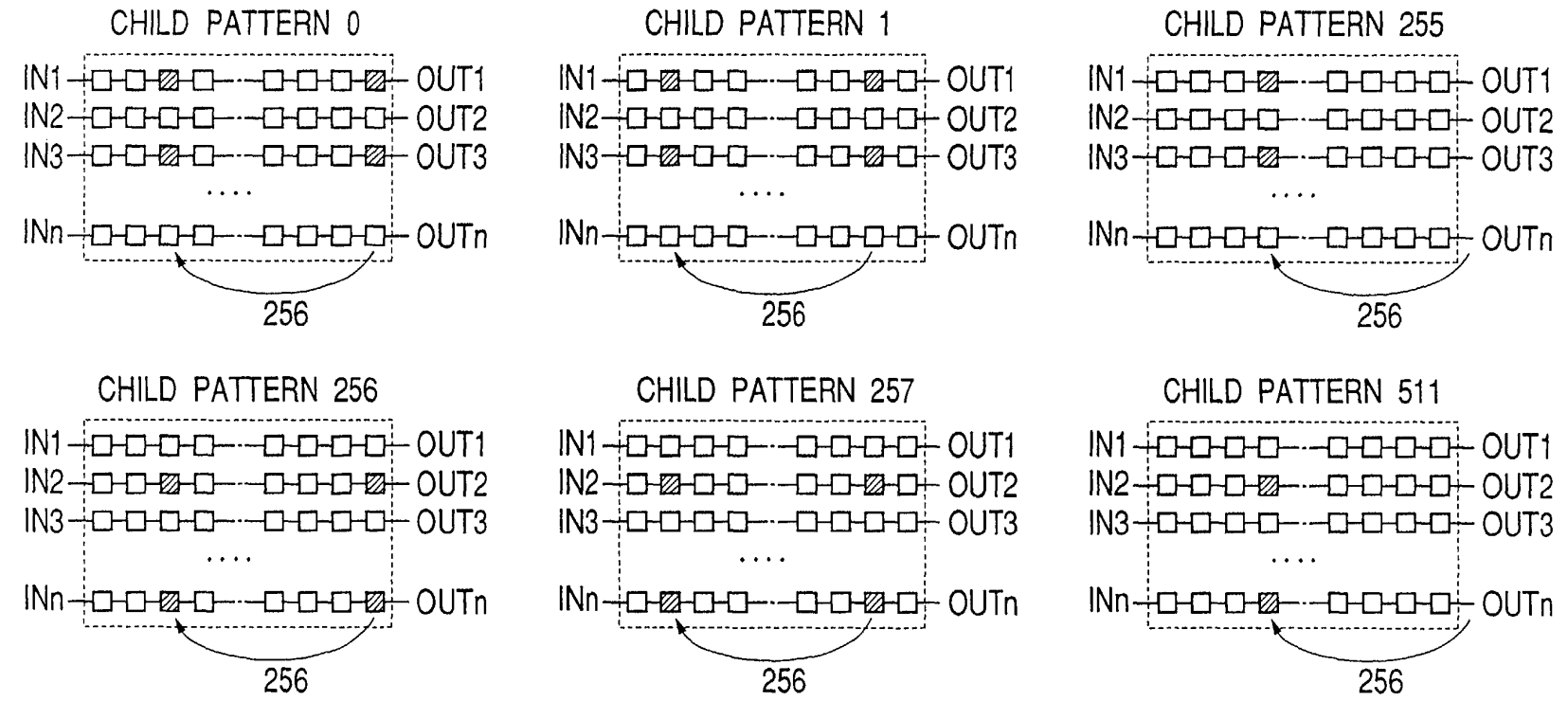

CHILD PATTERN 0
CHILD PATTERN 1
CHILD PATTERN 255
CHILD PATTERN 256
CHILD PATTERN 257
CHILD PATTERN 511
IN1
IN2
IN3
INn
OUT1
OUT2
OUT3
OUTn
256

FIG. 26

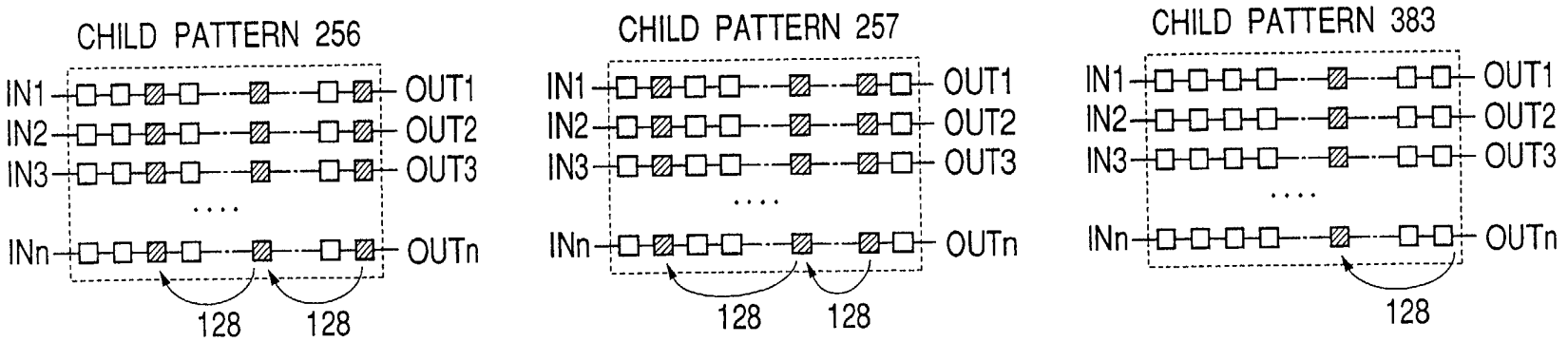

CHILD PATTERN 256
IN1
IN2
IN3
INn
OUT1
OUT2
OUT3
OUTn
128
128
CHILD PATTERN 257
IN1
IN2
IN3
INn
OUT1
OUT2
OUT3
OUTn
128
128
CHILD PATTERN 383
IN1
IN2
IN3
INn
OUT1
OUT2
OUT3
OUTn
128

FIG. 27

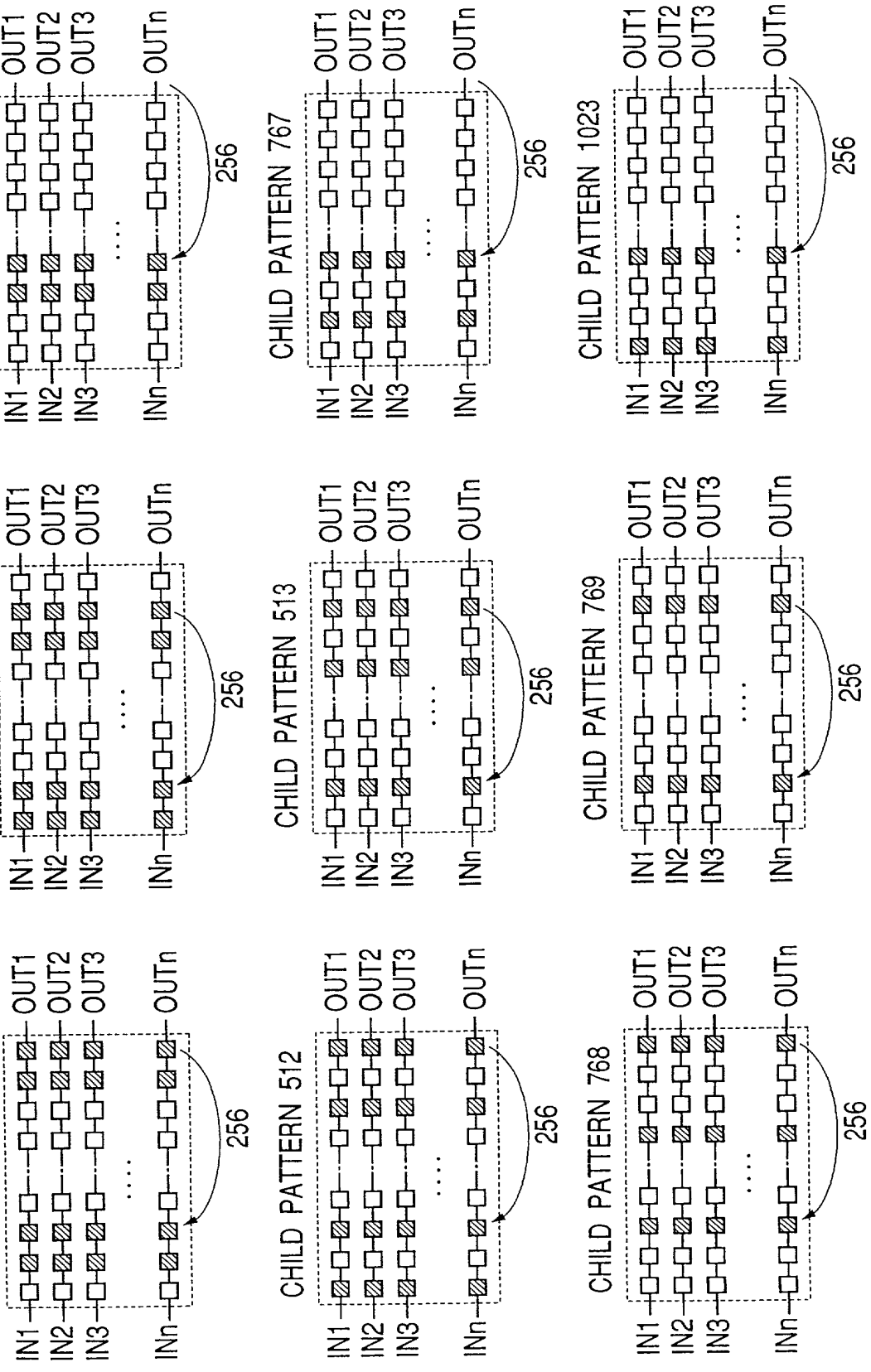

CHILD PATTERN 256
CHILD PATTERN 257
CHILD PATTERN 511
CHILD PATTERN 512
CHILD PATTERN 513
CHILD PATTERN 767
CHILD PATTERN 768
CHILD PATTERN 769
CHILD PATTERN 1023
IN1
IN2
IN3
INn
OUT1
OUT2
OUT3
OUTn
256

FIG. 28(a)

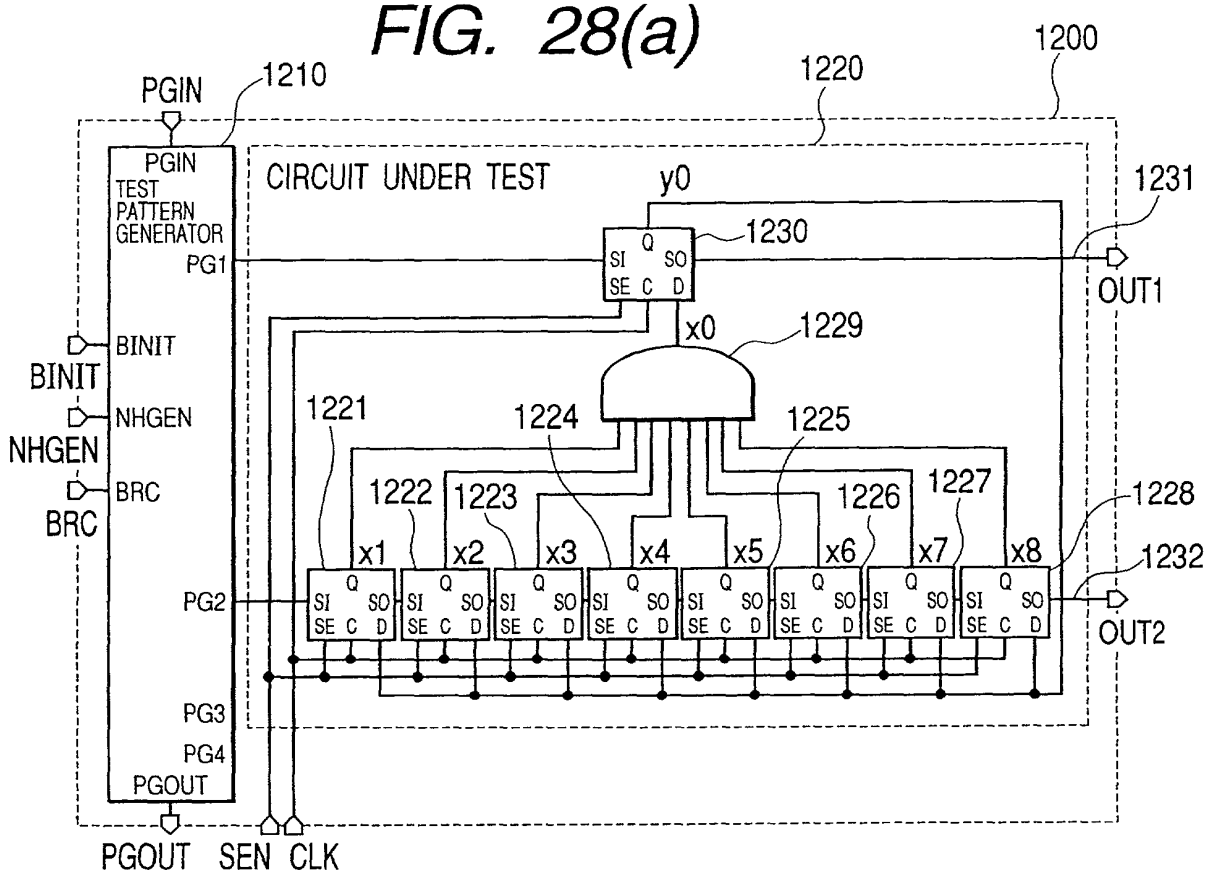


FIG. 28(b)

1241 PATTERN NUMBER	1242 TEST PATTERN x1	x2	x3	x4	x5	x6	x7	x8	x0	1243 DETECTABLE STUCK-AT FAULT (SIGNAL LINE NAME/STUCK VALUE)
1	1	1	1	1	1	1	1	1	X	x0/0 x1/0 x2/0 x3/0 x4/0 x5/0 x6/0 x7/0 x8/0
2	0	1	1	1	1	1	1	1	X	x0/1 x1/1
3	1	0	1	1	1	1	1	1	X	x0/1 x2/1
4	1	1	0	1	1	1	1	1	X	x0/1 x3/1
5	1	1	1	0	1	1	1	1	X	x0/1 x4/1
6	1	1	1	1	0	1	1	1	X	x0/1 x5/1
7	1	1	1	1	1	0	1	1	X	x0/1 x6/1
8	1	1	1	1	1	1	0	1	X	x0/1 x7/1
9	1	1	1	1	1	1	1	0	X	x0/1 x8/1
10	X	X	X	X	X	X	X	X	1	y0/0
11	X	X	X	X	X	X	X	X	0	y0/1

FIG. 29

TIME	MODE	BI NIT	NH GEN	BRC	SEN	CLK	TDI	FBI EN	PG1	PG2	PG3	PG4	LC1	LC2	LC3	HC1	HC2	HC3
0	INITIALIZATION	0	0	0	1	0	1	X	X	X	X	X	X	X	X	X	X	X
1		1	0	P	1	0	1	1	X	X	X	X	X	X	X	X	X	X
2		1	0	P	1	0	1	1	1	X	X	X	X	X	X	X	X	X
3		1	0	P	1	0	0	1	1	1	X	X	X	X	X	X	X	X
4		1	0	P	1	0	0	0	1	1	1	X	X	X	X	X	X	X
5		1	0	P	1	0	0	0	0	1	1	1	X	X	X	X	X	X
6		1	0	P	1	0	1	0	0	0	1	1	1	X	X	X	X	X
7		1	0	P	1	0	1	1	0	0	0	1	1	1	X	X	X	X
8		1	0	P	1	0	1	1	1	0	0	0	1	1	1	X	X	X
9		1	0	P	1	0	1	1	1	1	0	0	0	1	1	1	X	X
10		1	0	P	1	0	0	1	1	1	1	0	0	0	1	1	1	X
11		1	0	P	1	0	X	0	1	1	1	1	0	0	0	1	1	1
12	PARENT PATTERN SETTING	0	0	P	1	P	X	0	1	1	1	1	1	0	0	1	1	1
13		0	0	P	1	P	X	0	1	1	1	1	0	1	0	1	1	1
14		0	0	P	1	P	X	0	1	1	1	1	1	1	0	1	1	1
15		0	0	P	1	P	X	0	1	1	1	1	0	0	1	1	1	1
16		0	0	P	1	P	X	0	1	1	1	1	1	0	1	1	1	1
17		0	0	P	1	P	X	0	1	1	1	1	0	1	1	1	1	1
18		0	0	P	1	P	X	0	1	1	1	1	1	1	1	1	1	1
19		0	0	P	1	P	X	0	1	1	1	1	0	0	0	1	1	1
20	CLOCK ADVANCE	0	1	P	0	P	X	0	1	1	1	1	0	0	0	0	0	0
21	CHILD PATTERN 0 SETTING (RESULT OF PARENT PATTERN)	1	1	P	1	P	X	0	1	1	1	1	1	0	0	0	0	0
22		1	1	P	1	P	X	0	1	1	1	1	0	1	0	0	0	0
23		1	1	P	1	P	X	0	1	1	1	1	1	1	0	0	0	0
24		1	1	P	1	P	X	0	1	1	1	1	0	0	1	0	0	0
25		1	1	P	1	P	X	0	1	1	1	1	1	0	1	0	0	0
26		1	1	P	1	P	X	0	1	1	1	1	0	1	1	0	0	0
27		1	1	P	1	P	X	0	1	1	1	1	1	1	1	0	0	0
28		1	1	P	1	P	X	0	1	1	1	1	0	0	0	0	0	0
29	CLOCK ADVANCE	0	1	P	1	P	X	0	1	1	1	1	0	0	0	1	0	0
30	CHILD PATTERN 1 SETTING (RESULT OF CHILD PATTERN 0)	1	1	P	1	P	X	0	1	1	1	1	1	0	0	1	0	0
31		1	1	P	1	P	X	0	1	1	1	1	0	1	0	1	0	0
32		1	1	P	1	P	X	0	1	1	1	1	1	1	0	1	0	0
33		1	1	P	1	P	X	0	1	1	1	1	0	0	1	1	0	0
34		1	1	P	1	P	X	0	1	1	1	1	1	0	1	1	0	0
35		1	1	P	1	P	X	0	1	1	1	1	0	1	1	1	0	0
36		1	1	P	1	P	X	0	1	1	1	1	1	1	1	1	0	0
37		1	1	P	1	P	X	0	1	1	1	1	0	0	0	1	0	0
38	CLOCK ADVANCE	0	1	P	1	P	X	0	1	1	1	1	0	0	0	0	1	0
83	CLOCK ADVANCE	0	1	P	1	P	X	0	1	1	1	1	0	0	0	1	1	1
84	CHILD PATTERN 7 SETTING (RESULT OF CHILD PATTERN 6)	1	1	P	1	P	X	0	1	1	1	1	1	0	0	1	1	1
85		1	1	P	1	P	X	0	1	1	1	1	0	1	0	1	1	1
86		1	1	P	1	P	X	0	1	1	1	1	1	1	0	1	1	1
87		1	1	P	1	P	X	0	1	1	1	1	0	0	1	1	1	1
88		1	1	P	1	P	X	0	1	1	1	1	1	0	1	1	1	1
89		1	1	P	1	P	X	0	1	1	1	1	0	1	1	1	1	1
90		1	1	P	1	P	X	0	1	1	1	1	1	1	1	1	1	1
91		1	1	P	1	P	X	0	1	1	1	1	0	0	0	1	1	1
92	CLOCK ADVANCE	0	1	P	1	P	X	0	1	1	1	1	0	0	0	0	0	0
93	RESULT OF CHILD PATTERN	1	1	P	1	P	X	0	1	1	1	1	1	0	0	0	0	0
94		1	1	P	1	P	X	0	1	1	1	1	0	1	0	0	0	0
95		1	1	P	1	P	X	0	1	1	1	1	1	1	0	0	0	0
96		1	1	P	1	P	X	0	1	1	1	1	0	0	1	0	0	0
97		1	1	P	1	P	X	0	1	1	1	1	1	0	1	0	0	0
98		1	1	P	1	P	X	0	1	1	1	1	0	1	1	0	0	0
99		1	1	P	1	P	X	0	1	1	1	1	1	1	1	0	0	0
100		1	1	P	1	P	X	0	1	1	1	1	1	1	1	0	0	0

FIG. 30

TIME	MODE	y0	x1	x2	x3	x4	x5	x6	x7	x8	o1	o2
0	INITIALIZATION	X	X	X	X	X	X	X	X	X	X	X
1		X	X	X	X	X	X	X	X	X	X	X
2		X	X	X	X	X	X	X	X	X	X	X
3		X	X	X	X	X	X	X	X	X	X	X
4		X	X	X	X	X	X	X	X	X	X	X
5		X	X	X	X	X	X	X	X	X	X	X
6		X	X	X	X	X	X	X	X	X	X	X
7		X	X	X	X	X	X	X	X	X	X	X
8		X	X	X	X	X	X	X	X	X	X	X
9		X	X	X	X	X	X	X	X	X	X	X
10		X	X	X	X	X	X	X	X	X	X	X
11		X	X	X	X	X	X	X	X	X	X	X
12	PARENT PATTERN SETTING	1	1	X	X	X	X	X	X	X	X	X
13		1	1	1	X	X	X	X	X	X	1	X
14		1	1	1	1	X	X	X	X	X	1	X
15		1	1	1	1	1	X	X	X	X	1	X
16		1	1	1	1	1	1	X	X	X	1	X
17		1	1	1	1	1	1	1	X	X	1	X
18		1	1	1	1	1	1	1	1	X	1	X
19		1	1	1	1	1	1	1	1	1	1	X
20	CLOCK ADVANCE	1	1	1	1	1	1	1	1	1	1	X
21	CHILD PATTERN 0 SETTING (RESULT OF PARENT PATTERN)	0	0	1	1	1	1	1	1	1	1	1
22		1	1	0	1	1	1	1	1	1	0	1
23		1	1	1	0	1	1	1	1	1	1	1
24		1	1	1	1	0	1	1	1	1	1	1
25		1	1	1	1	1	0	1	1	1	1	1
26		1	1	1	1	1	1	0	1	1	1	1
27		1	1	1	1	1	1	1	0	1	1	1
28		1	1	1	1	1	1	1	1	0	1	1
29	CLOCK ADVANCE	0	1	1	1	1	1	1	1	1	1	1
30	CHILD PATTERN 1 SETTING (RESULT OF CHILD PATTERN 0)	1	1	1	1	1	1	1	1	1	0	1
31		0	0	1	1	1	1	1	1	1	1	1
32		1	1	0	1	1	1	1	1	1	1	1
33		1	1	1	0	1	1	1	1	1	1	1
34		1	1	1	1	0	1	1	1	1	1	1
35		1	1	1	1	1	0	1	1	1	1	1
36		1	1	1	1	1	1	0	1	1	1	1
37		1	1	1	1	1	1	1	0	1	1	1
38	CLOCK ADVANCE	0	1	1	1	1	1	1	1	1	1	1
83	CLOCK ADVANCE	0	1	1	1	1	1	1	1	1	1	1
84	CHILD PATTERN 7 SETTING (RESULT OF CHILD PATTERN 6)	1	1	1	1	1	1	1	1	1	0	1
85		1	1	1	1	1	1	1	1	1	1	1
86		1	1	1	1	1	1	1	1	1	1	1
87		1	1	1	1	1	1	1	1	1	1	1
88		1	1	1	1	1	1	1	1	1	1	1
89		1	1	1	1	1	1	1	1	1	1	1
90		1	1	1	1	1	1	1	1	1	1	1
91		0	0	1	1	1	1	1	1	1	1	1
92	CLOCK ADVANCE	0	0	0	0	0	0	0	0	0	1	1
93	RESULT OF CHILD PATTERN	0	0	0	0	0	0	0	0	0	0	0
94		1	1	0	0	0	0	0	0	0	1	0
95		1	1	1	0	0	0	0	0	0	1	0
96		1	1	1	1	0	0	0	0	0	1	0
97		1	1	1	1	1	0	0	0	0	1	0
98		1	1	1	1	1	1	0	0	0	1	0
99		1	1	1	1	1	1	1	0	0	1	0
100		1	1	1	1	1	1	1	1	0	1	0

FIG. 31(a)

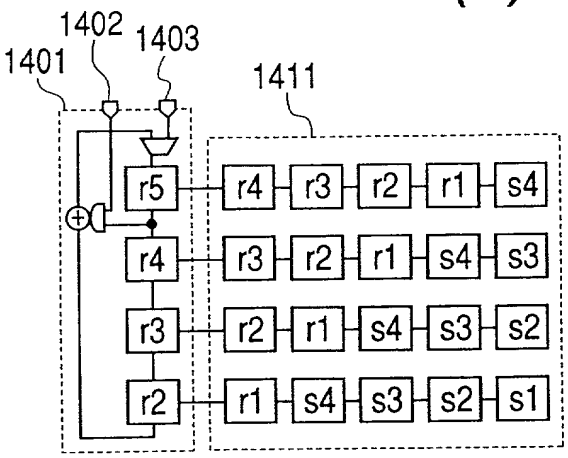


FIG. 31(b)

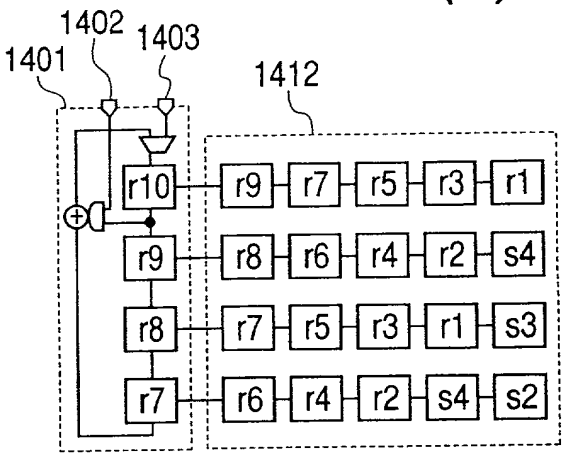


FIG. 31(c)

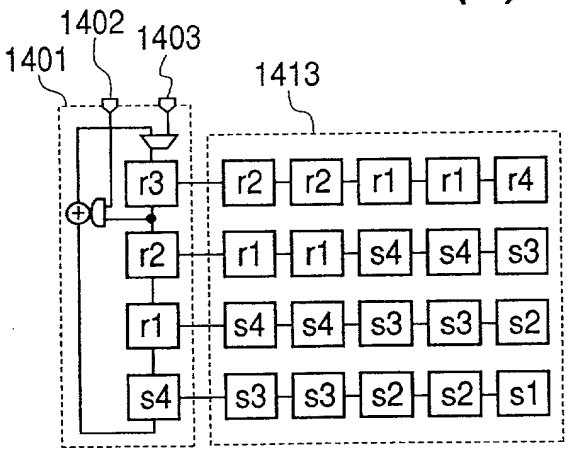


FIG. 31(d)

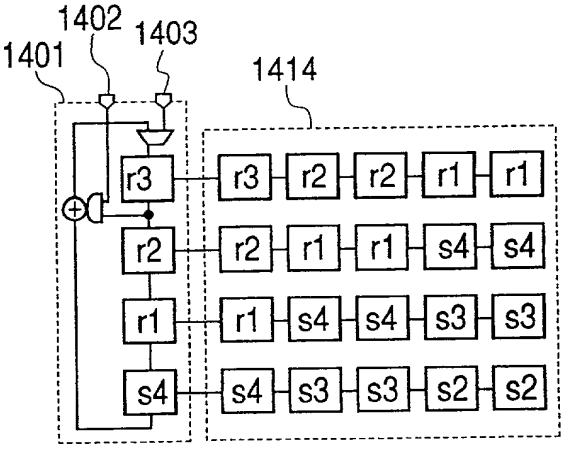


FIG. 31(e)

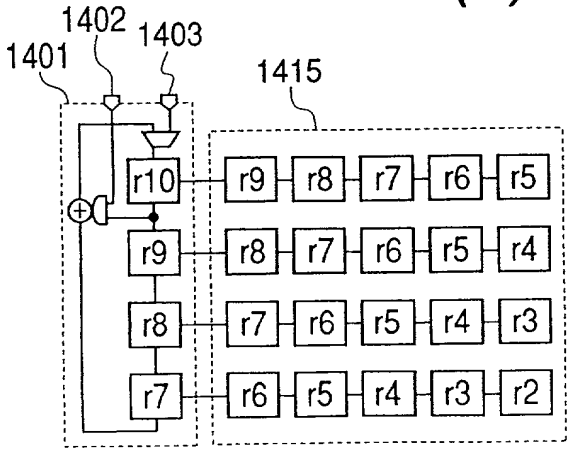


FIG. 32(a)

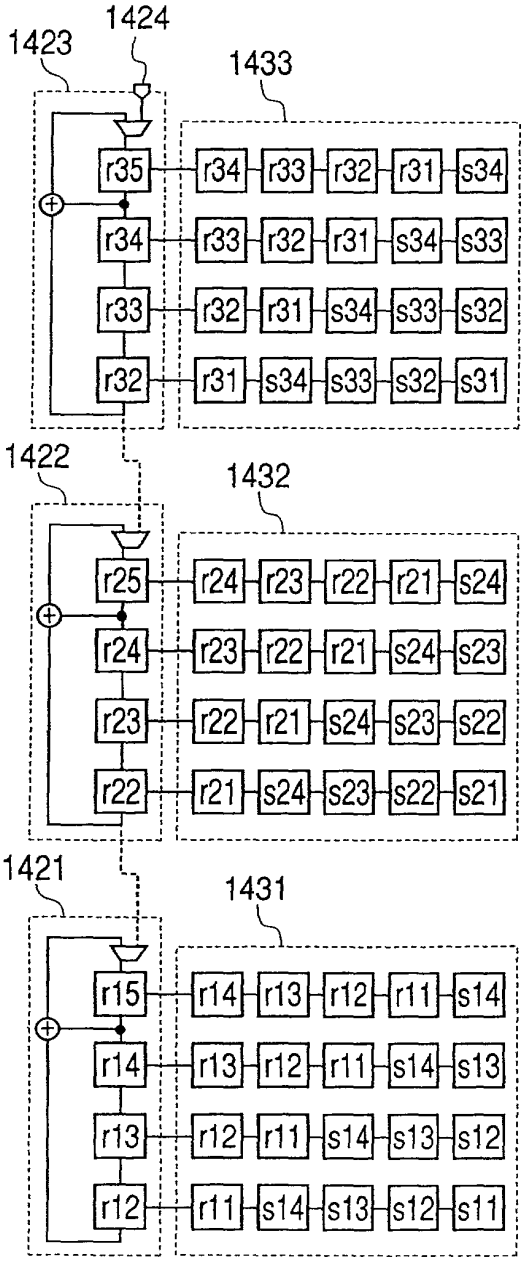


FIG. 32(b)

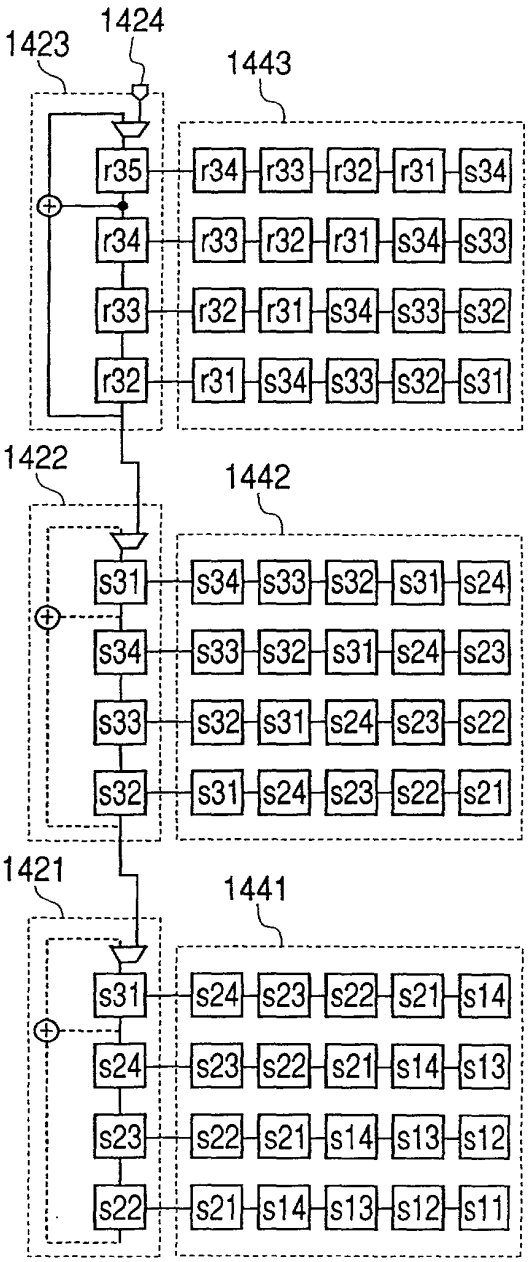


FIG. 33

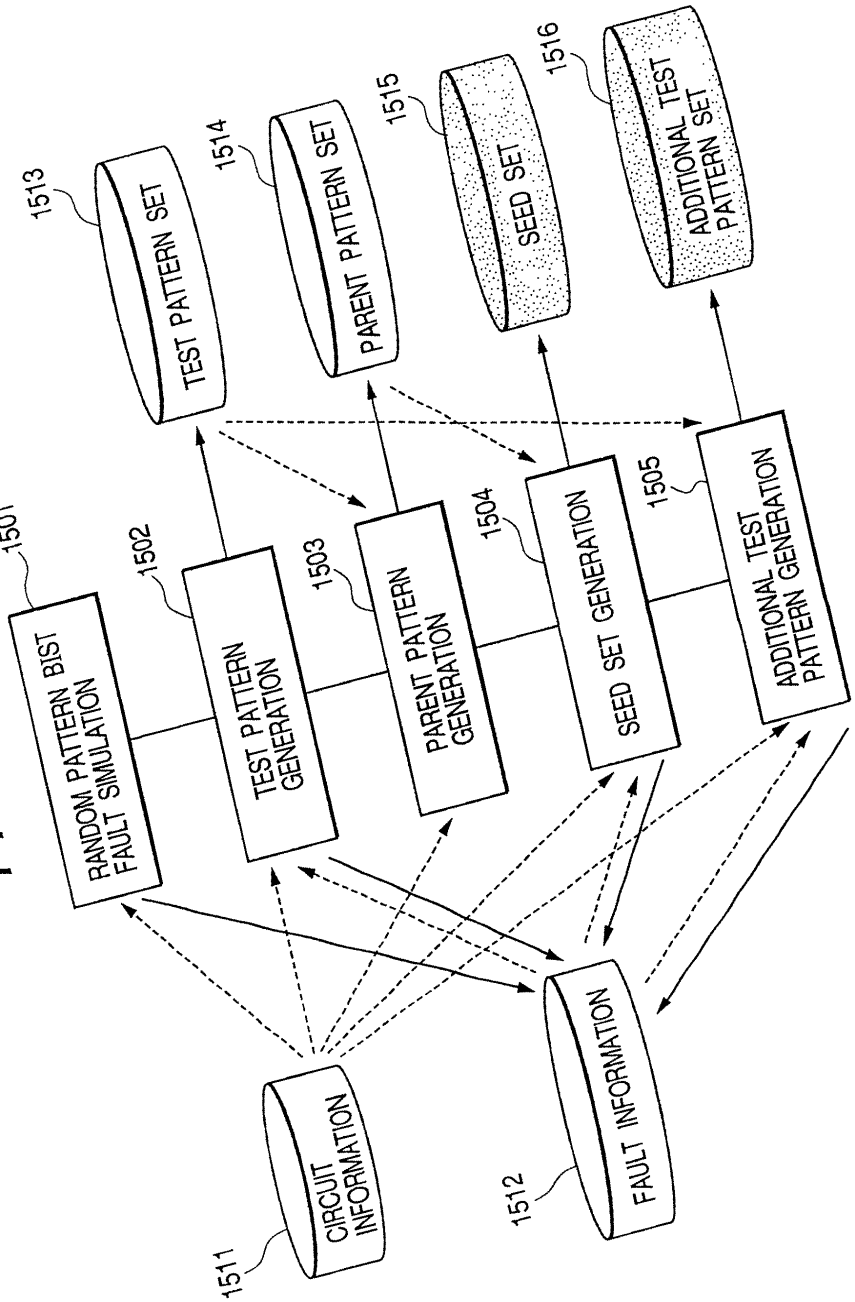

1501
RANDOM PATTERN BIST FAULT SIMULATION
1502
TEST PATTERN GENERATION
1503
PARENT PATTERN GENERATION
1504
SEED SET GENERATION
1505
ADDITIONAL TEST PATTERN GENERATION
1511
CIRCUIT INFORMATION
1512
FAULT INFORMATION
1513
TEST PATTERN SET
1514
PARENT PATTERN SET
1515
SEED SET
1516
ADDITIONAL TEST PATTERN SET

FIG. 34

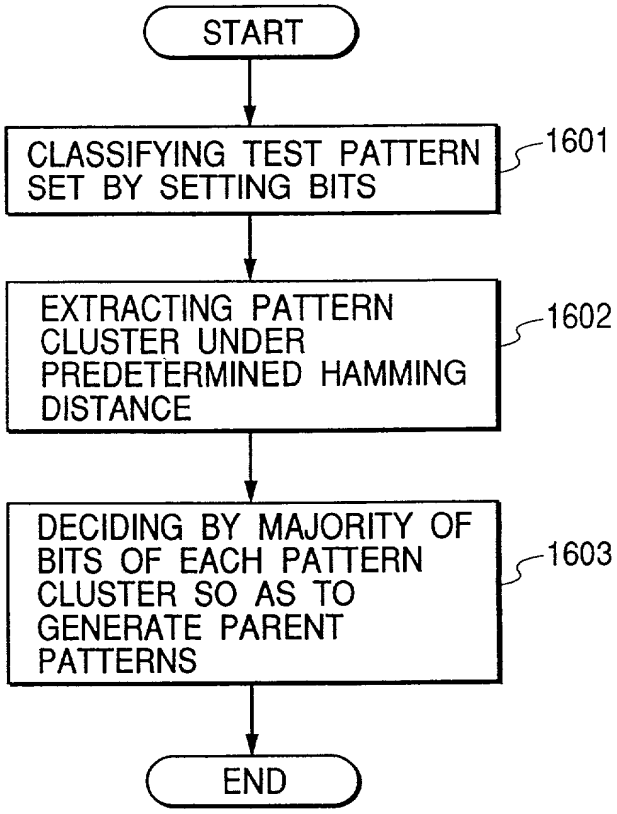

START
CLASSIFYING TEST PATTERN SET BY SETTING BITS
1601
EXTRACTING PATTERN CLUSTER UNDER PREDETERMINED HAMMING DISTANCE
1602
DECIDING BY MAJORITY OF BITS OF EACH PATTERN CLUSTER SO AS TO GENERATE PARENT PATTERNS
1603
END

FIG. 35

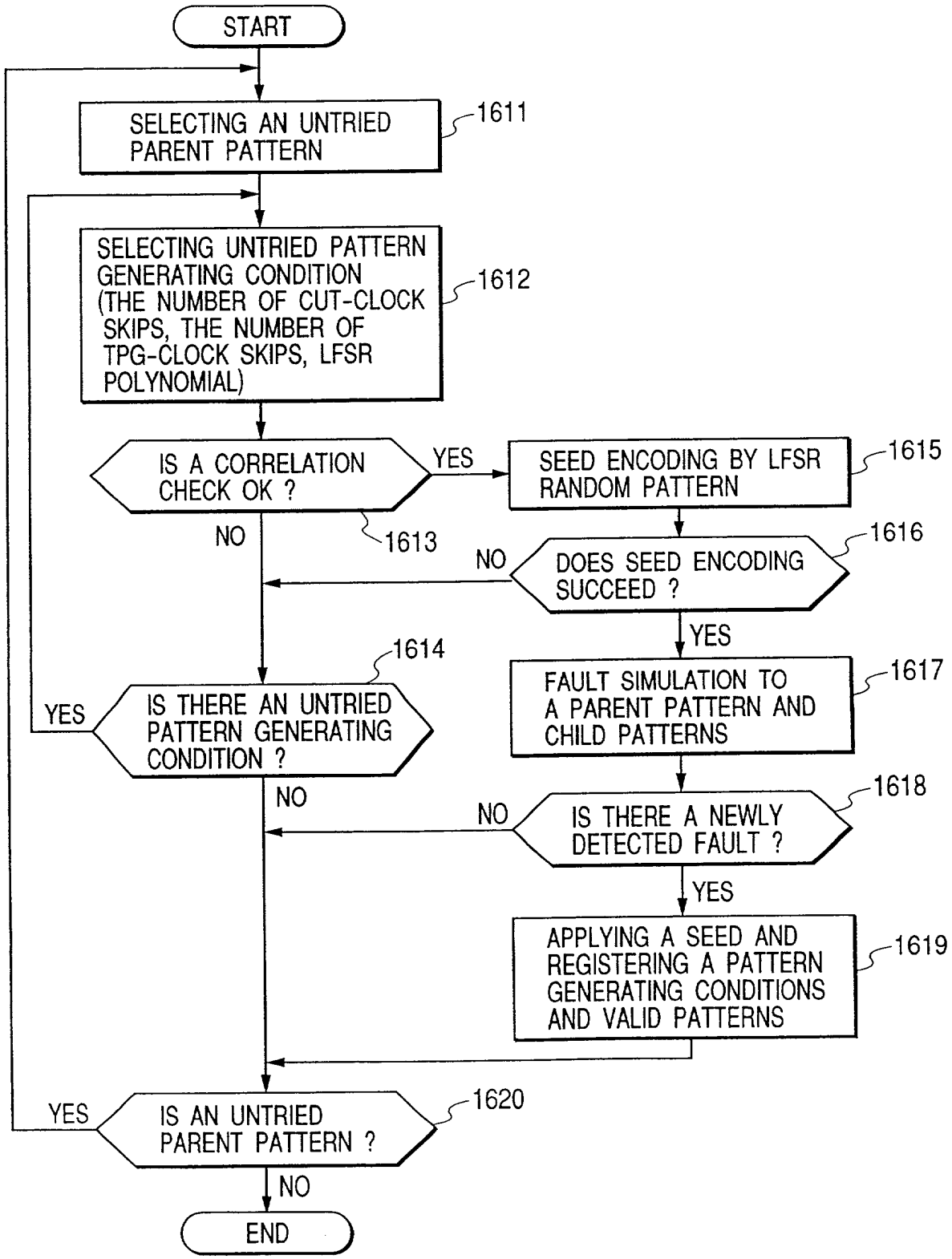

START
SELECTING AN UNTRIED PARENT PATTERN
1611
SELECTING UNTRIED PATTERN GENERATING CONDITION (THE NUMBER OF CUT-CLOCK SKIPS, THE NUMBER OF TPG-CLOCK SKIPS, LFSR POLYNOMIAL)
1612
IS A CORRELATION CHECK OK ?
YES
SEED ENCODING BY LFSR RANDOM PATTERN
1615
NO
1613
NO
DOES SEED ENCODING SUCCEED ?
1616
YES
1614
FAULT SIMULATION TO A PARENT PATTERN AND CHILD PATTERNS
1617
YES
IS THERE AN UNTRIED PATTERN GENERATING CONDITION ?
NO
NO
IS THERE A NEWLY DETECTED FAULT ?
1618
YES
APPLYING A SEED AND REGISTERING A PATTERN GENERATING CONDITIONS AND VALID PATTERNS
1619
YES
IS AN UNTRIED PARENT PATTERN ?
1620
NO
END

FIG. 36

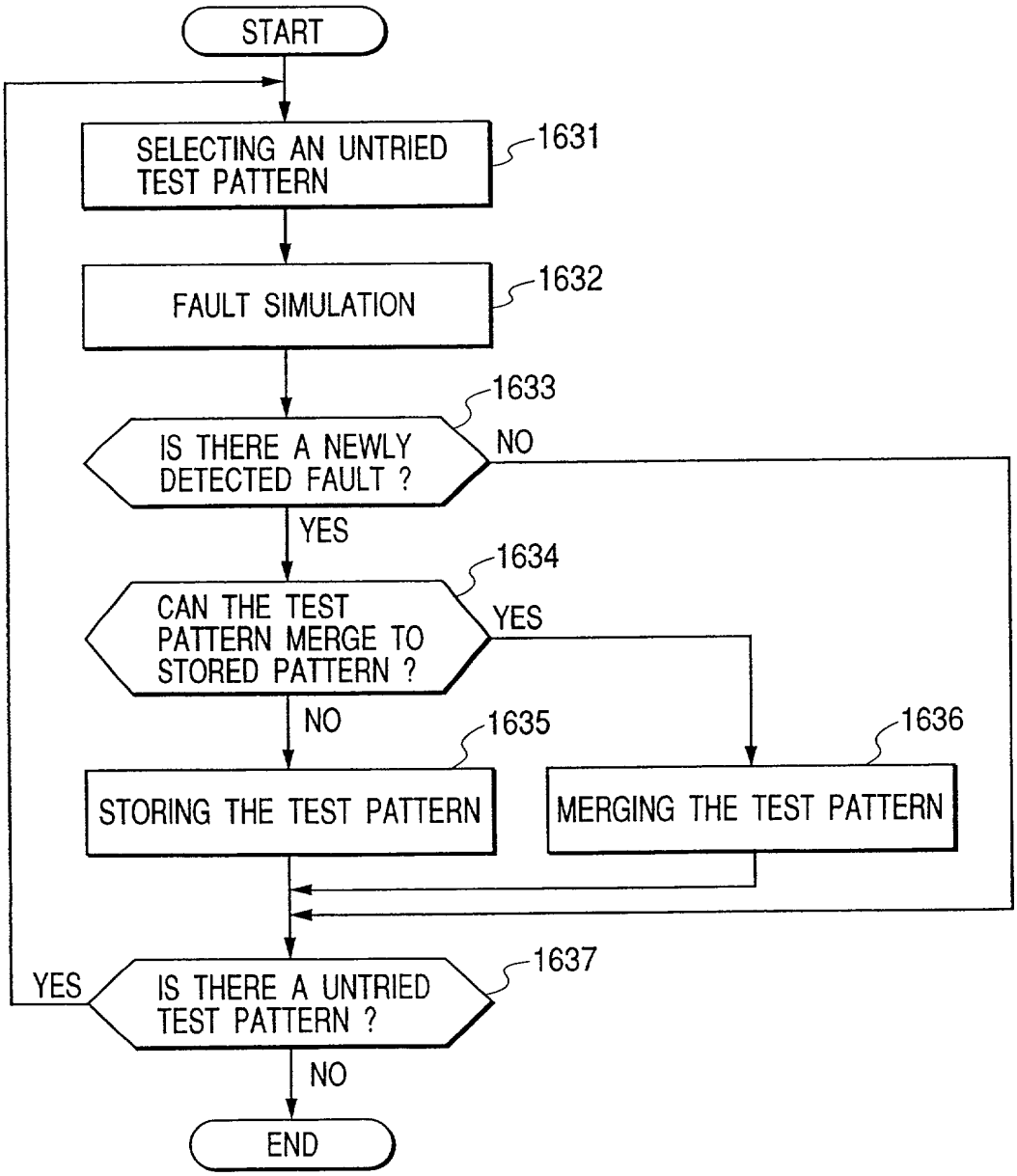

START
SELECTING AN UNTRIED TEST PATTERN
1631
FAULT SIMULATION
1632
1633
IS THERE A NEWLY DETECTED FAULT ?
NO
YES
1634
CAN THE TEST PATTERN MERGE TO STORED PATTERN ?
YES
NO
1635
1636
STORING THE TEST PATTERN
MERGING THE TEST PATTERN
1637
YES
IS THERE A UNTRIED TEST PATTERN ?
NO
END

FIG. 37

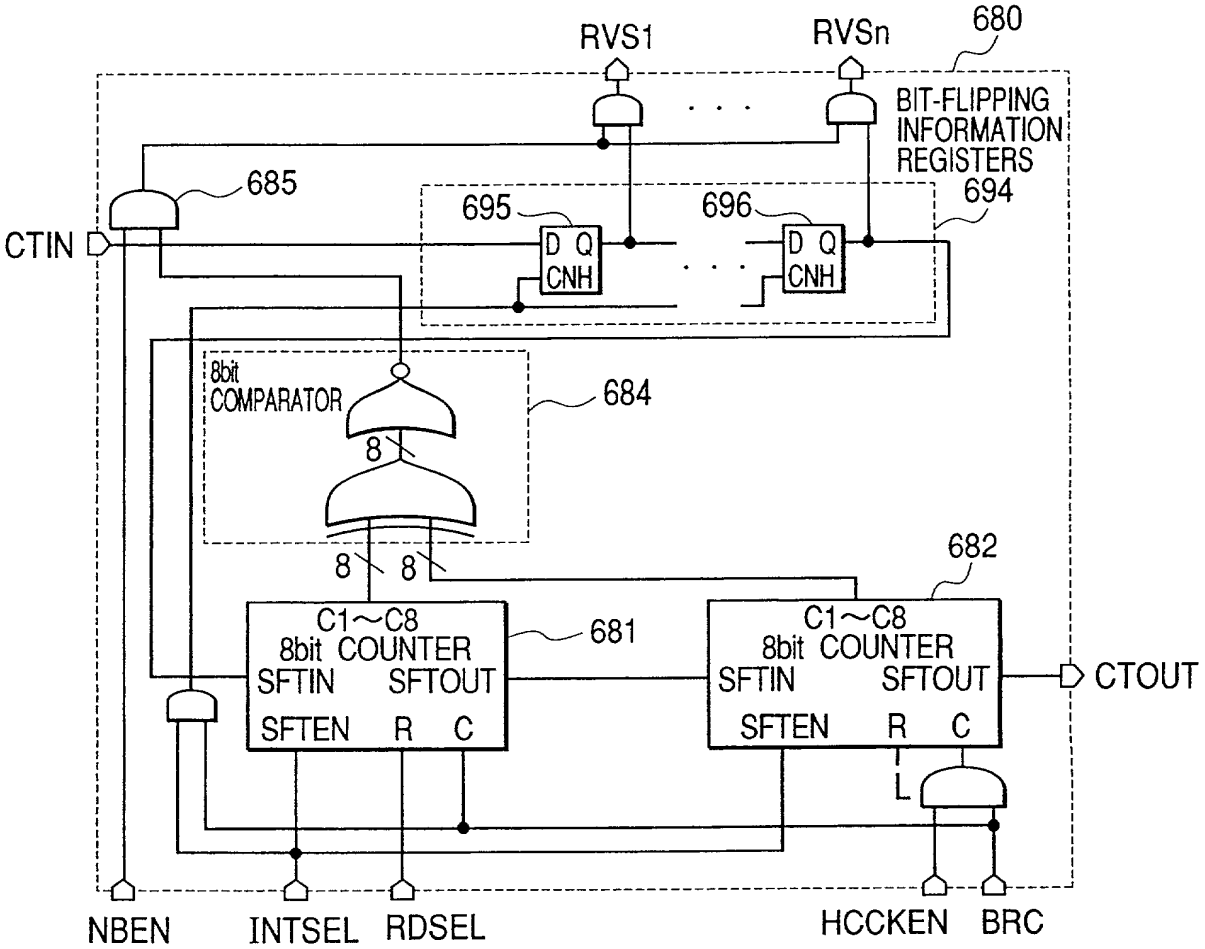
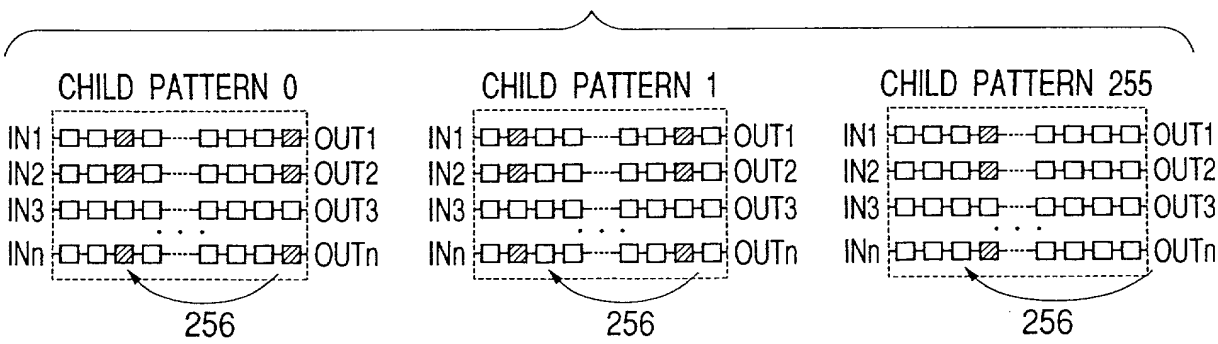

RVS1
RVSn
680
BIT-FLIPPING INFORMATION REGISTERS
694
685
695
696
D Q
CNH
CTIN
8bit COMPARATOR
684
8
8
8
682
C1~C8
8bit COUNTER
SFTIN
SFTOUT
SFTEN
R
C
681
CTOUT
L
NBEN
INTSEL
RDSEL
HCCKEN
BRC

FIG. 38


CHILD PATTERN 0
CHILD PATTERN 1
CHILD PATTERN 255
IN1
IN2
IN3
INn
OUT1
OUT2
OUT3
OUTn
256